

Process Makes Electroless Nickel/Gold Wafer Bumping Economical for Flip-Chip Packaging

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Flip-chip technology is a driving force in achieving increased speed and performance along with higher I/O count for a variety of applications. This article discusses a low-cost wafer-level bumping process based on electroless nickel/gold (Ni/Au) under-bump metallization (UBM) that is suitable for all current flip-chip interconnection technologies.

Today, all commercially viable flip-chip methods require that a bump formation be placed on the chip I/O to act as the interconnection. Established techniques, however, like the C4 process(1,2) do not answer the cost requirements for the consumer market.

Alternatively, a selective chemical plating method can significantly reduce costs associated with bumping, since this method does not require masking or metal sputtering. Additionally, this technology enables the parallel processing of multiple wafers, resulting in high throughput.



Figure 1. Fifty 200mm wafers are shown undergoing parallel batch processing.

A cost-effective bumping and assembly process that employs solder stencil printing or direct assembly with ACF or NCP adhesives can also be achieved. (Figure 1 shows a batch of wafers being processed in parallel).

Cost Savings

With the emergence of 300mm wafers, electroless and maskless processes provide basic advantages and cost savings, because their use requires slight or no additional investment.

Additionally, this electroless bumping process presents new possibilities for the manufacture of semiconductors. Because wire bonding onto copper pads is impossible, electroless Ni/Au enables the use of low-cost metallization of copper pads suited for wire bonding.



Figure 2. Process flow for electroless Ni/Au deposition on

wafers up to 300mm

Wafer-Level Redistribution

Electroless Ni/Au processes work well for low-cost wafer-level redistribution and wafer-level packaging when combined with additive or semi-additive wafer-level processes. (Figure 2 shows a process flow for the wafer-level CSP and a low-cost redistribution process based on electroless Ni/Au bumping and semi-additive electroless copper plating on a special dielectric.(3))

The electroless bumping of 300mm wafers allows specific cost savings, because more established 300mm equipment processes demand photo-imaging, requiring costly steppers and 300mm sputtering and plating equipment.

By contrast, electroless Ni/Au bumping requires only specially adapted wafer-bumping tanks for the chemical process. Moreover, the dollar investment for the process may be 5-10 times less than the cost to establish a standard electroplating process.

During flip-chip assembly, the Ni/Au bumps protect the Al and act as both an adhesion layer and a diffusion barrier, providing a stable and reliable contact to the aluminum bond pads.(4,5) Additionally, the Ni can also serve as a standoff for chip-on-glass using isotropic conductive adhesive ACF or NCP.(6)

The feasibility and reliability of this bumping process has been established in a series of published technical papers.(7,8) (Figure 3 shows electroless Ni/Au as a basis for an ACF flip-chip assembly, polymeric flip-chip assembly (conductive adhesive) and for soldering and DCA applications with different solder alloys.)

State-of-the-Art

Chemical Ni/Au bumping is a wet-chemical and maskless process. With this well-established manufacturing process, all wafer types can be bumped with a standard process and will result in excellent quality. Using a specially designed bumping line, wafers from 100mm to 300mm in diameter can be plated.

The basic electroless nickel bumping process can be performed with standard, available chemicals for simple test structures/test dies without inner circuitry.

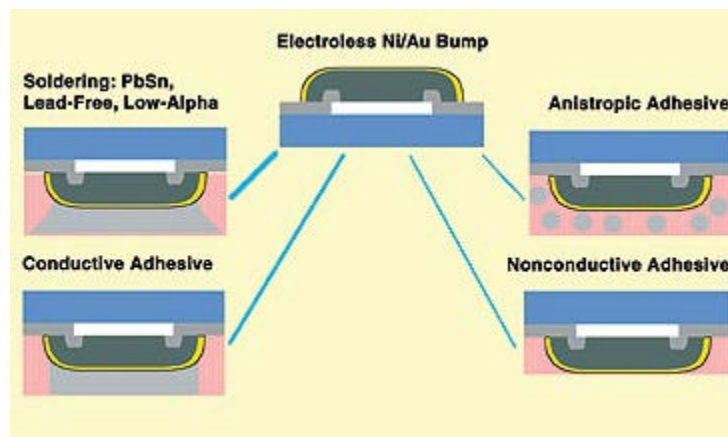


Figure 3. Electroless Ni/Au under-bump metallization can be employed for flip-chip assembly processes.

When applied to functional wafers with complex inner electrical structures, different metallization, and different passivations, however, the process requires specific proprietary chemical compositions and know-how to achieve reproducible and reliable result.

Electroless nickel is employed in industry for a wide range of applications in which aluminum work pieces are plated with nickel. The equipment available for these standard processes, based on large work pieces or PC boards, is unsuitable for wafer bumping.

Modular Wafer Bumping Line

To meet the specific requirements for wafer bumping, a modular electroless nickel wafer bumping line, The PacLine2000, has been developed. Each module can process batches of fifty 200mm or twenty-five 300mm wafers. Automated wafer handling and processing were implemented in the system for higher throughput. (Figure 4 shows the 300mm equipment with wafer loader, reloader and robot handling systems.)

Throughput is governed by the desired thickness of electroless Ni/Au. For UBM, 5µm nickel is typically required. The average processing time is 20 minutes, which translates to one-hundred-fifty 200mm or seventy-five 300mm wafers per hour. Optical microscopy, profilometer measurements and shear tests verify bump quality.

The minimum bump height is 1µm for a closed and voidless nickel layer, because the pad-to-pad spacing limits the maximum height.

The bump height must not be larger than one-half the pad spacing minus 5µm to avoid short circuits between neighboring pads by overgrowing nickel. A UBM height of 5µm is recommended for flip-chip soldering. (The Ni/Au bump characteristics are summarized in Table 1. Table 2 compares solder bumping methods.)

Table 1. Ni/Au Bump Characteristics	
Bump Characteristic	Specification
Recommended height for FC soldering	5µm
Maximum height	=1/2 pad spacing -5µm
Material	NiP 10%
Resistivity	70 µOcm
Hardness	550 mHV
Adhesion to Al 100x100 µm ² pad	>100g (typ.150g)
Au coating thickness	0.05 – 0.5µm

Design rules(9) have been defined for achieving reliable and reproducible results using electroless Ni/Au bumping of several types of wafers from 100mm to 1300mm, as pad materials AlSi 1%, AlSi 1% Cu 0.5%, AlCu 2% and other alloys of these metals were investigated.

Table 2. Attributes of Various Solder Bumping Techniques

	Electroplating	Stencil Printing	Laser Jetting
Tooling Requirement	Mask	Stencil	None
Capital Cost	Very High	Medium	Low
Equipment	1. Sputtering 2. Mask Aligner 3. Plating Tool 4. Reflow Oven	1. Printer 2. Reflow Oven 3. Flux Cleaning	1a. SB2-SM or 1b. SB2-Jet
Throughput	High	Very High	Medium
Flux	No	Yes	No
Local Reflow	No	No	Yes
Mechanical Contact	Yes	Yes	No
3D Packaging	No	No	Yes
Solder Alloy Flexibility	Low	Medium	High

All bump types have been processed with acceptable results; nevertheless, there are some restrictions on the wafers to be nickel bumped. The aluminum bond-pad thickness should be 0.8 μ m or more in order to have sufficient Al after cleaning and activation. There are no limits to passivation thickness, but the passivation must be defect-free.

Cracks cause a growth of nickel that may produce a short circuit. This will also occur on parts of a wafer surface that were scratched by improper handling. Nickel also grows on silicon that is not covered by an oxide or passivation.

Die Attach

As alternatives to adhesive assembly techniques, the use of a tall Ni/Au bump and ACF or NCP standard solder reflow processes represent the most important die attach methods.(10)

Ni/Au UBM is very flexible for use with different 300mm-capable soldering processes and applications. When electroless Ni/Au is combined with solder stencil printing, and solder paste is deposited through a metal stencil, an attractive solder bumping process results.

Typical solder pastes include Pb37Sn63 alloys with particle sizes below 20 μ m. Low-alpha solder pastes with particle counts below 0.002cph/cm² are also available.



Figure 4. PacLine 2000 for 300mm wafers

Another interesting possibility for applying solder bumps on a wafer is by attaching preformed solder balls. This attachment can be achieved with a solder gang-placement method.

Today's demands for packaging of optoelectronics and MEMS devices can no longer be met with standard, flux-based processes that use a long-duration temperature reflow

profile and require excessive mechanical handling steps.

These devices require fluxless soldering and no thermal stresses or mechanical contact, which could damage sensitive membranes in MEMS or optical components. Some applications, moreover, require 3D packaging and selective solder applications in 3D structures. These specific needs can be met, however, by a laser-based solder jetting technology.

Summary

In summary, the electroless Ni/Au bumping process, especially when employed to process 300mm wafers, offers a powerful roadmap for flip-chip interconnections in consumer products. The main challenge to electroless Ni/Au as a UBM in the near future is the reduction of pitches to below 50µm.

The development of solder application techniques, such as ball placement in this fine-pitch area, will continue. In addition, the trend toward lead-free or low-alpha solders for stencil printing will continue. An additional challenge will be a strategy of implementing test and known-good die in a process flow for electroless Ni/Au bumping.

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