

LAPLACE – A New Assembly Method using Laser Heating for Ultra Fine Pitch Devices

T. Teutsch, R. G. Blankenhorn, G. Azdasht*, P. Penke* and E. Zakel*

Pac Tech USA – Packaging Technologies, Inc.
328 Martin Avenue, Santa Clara, CA 95050
Phone: (408) 588-1925
Fax: (408) 588-1927
e-mail: teutsch@pactech-usa.com
www.pactech-usa.com

***Pac Tech – Packaging Technologies GmbH**
Am Schlangenhorst 15 -17, Germany
Phone: +49 (0)3321/4495 –0
Fax: +49 (0)3321/4495 –23
e-mail: zakel@pactech.de
www.pactech.de

J.-D. Kim, Y.-N. Kim, J.-W. Lee, J.-H. Park, H.-G. Kim and J.-O. Kim

**Semiconductor Material R&D Team,
Precision Instruments R&D Center, Samsung Techwin Co. Ltd
San14, Nongseo-Ri, Gigeung-Eub, Yongin-Si, Kyoungki -Do, 449-712, South Korea
Phone: +82-31-280-8068
e-mail: Jd95.kim@samsung.com
www.samsungtechwin.com**

Abstract

Established Flip-Chip assembly processes for LCD driver devices consist of a rather complex process flow due to different requirements in the combined placement of the large LCD devices and the small, multiple passive components all implemented in a standard LCD driver module. On a flex substrate the ultra fine pitch LCD chips are usually assembled by an adhesive process, the low I/O count passive devices are assembled using a solder reflow process.

A new and highly flexible assembly process approach using laser heating is introduced and the highly innovative Flip-Chip bonder system LAPLACE (LAsErPLACEr) is presented.

Compared to standard solder reflow or thermode bonding procedures one advantage of the LAPLACE system is the thermal and mechanical stress reduction by heating with laser pulses of a few millisecond duration which are coupling directly into the chip. Additionally common alignment problems due to different thermal expansion behavior of substrate and chip are reduced.

Process cycle times are improved by the equipment concept of performing chip pre alignment, placement and assembly reflow simultaneously and the absence of long heating and cooling cycles of standard thermode FC bonder systems. Especially, in combination with electroless Nickel UBM a dramatic cost reduction of the overall assembly process can be achieved. Beside this the process capability for ACF, NCP and solder interconnection techniques illustrates the high flexibility of the LAPLACE system.

New assembly results on pre-production scale using NCP and ACF materials together with sample analysis by cross sectioning and SEM are shown and a turnkey solution of a LCD driver assembly line is presented. Finally an outlook on the usage of the LAPLACE system for other applications and fluxless soldering is given.

I. Introduction

The use of lasers for soldering and microwelding is offering many technological advantages compared to the standard oven reflow or thermode soldering/ bonding methods.¹ The advantages are based on the laser physics, which offers the possibility of localized heat and short laser pulses. Localized heat means that no or minimal thermal stress is applied on the area outside of the bonding interface.

A short pulse leads to a low thermal stress on chip and substrate, respectively on the interconnections because the amount of thermal energy provided in one laser pulse is transferred in a short period of time. By laser, the heat is localized and the temperature can be applied selectively in the interconnection areas. It is not necessary to heat up a whole substrate to a reflow temperature in order to melt and reflow a small interconnection of a few μm size.^{2,3,4}

One technical advantages deduced from the use of laser physics is the compatibility with soldering and adhesive processes for flip chip attach.⁵ Lasers can be used for both – soldering, but also adhesive curing. This allows shorter soldering times and shorter adhesive curing times, significantly below one second.

Laser soldering and interconnection technology can also be applied for flip chip and resistor attach, as well as for solder attach. Lasers permit a high flexibility on substrate selections; especially allow bonding and soldering on low cost T_G - substrates that can be organic or inorganic material, rigid or flexible materials.

A comparison of the soldering times and soldering temperatures between SMT – oven reflow, thermode reflow and laser soldering is given in **Table 1**.

	Heating Time [sec]	Range [~]
Laser	0.01 – 0.1	msec
Thermode	2 - 4	sec
Reflow Oven	30 - 60	min

Table 1: Heating Time to Bonding Temperature for Solder Application

Figure 1 shows the schematics of the pulse time and thermal mode.

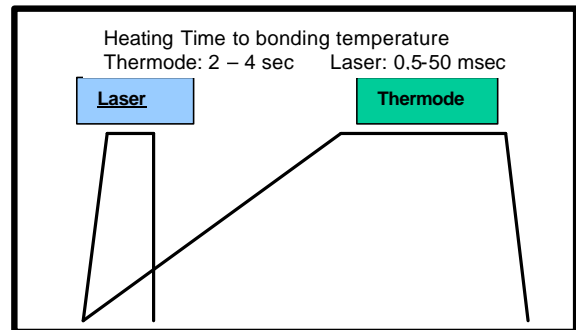


Figure1: Thermode Bonding vs. Laser Bonding

A comparison of the Flip Chip Adhesive Joining Processes is shown in **Table 2**. In contrast to soldering, adhesive joining allows a significant reduction of the interconnection temperature. However, the disadvantage of adhesive joining is a stronger dependence on the materials, since the interconnection is done by the adhesive material itself. Generally longer processing times because the curing of the adhesive material must be calculated during the Flip Chip Assembly operation.

Laser Curing allows a significant reduction in the processing times in the range of milliseconds, since the temperature which can be induced in a short time is significantly higher compared to a thermode or oven curing.

Flip Chip Assembly Processes		
• Adhesive joining		
– ACA	150-180° C	5-20 sec
• anisotropic conductive adhesive		
– ICA	50-100° C	300- 600 sec
• isotropic conductive adhesive		
– NCA	150-180° C	5- 20 sec
• nonconductive adhesive		
– Laser curing	150-300° C	< 1 sec

Table 2: Comparison of the Flip Chip Adhesive Joining Processes

An overview on the substrate materials used in today's Flip Chip applications is given in **Table 3**.

Substrates Capable for LAPLACE	
Rigid	FR4, BT-Epoxy, Polyimide, Ceramic, TG, Silicon
Flex	Polyimide, PP, PVC

Table 3: Substrate Materials

The technology is compatible with all standard processes used in industry today. Of course, basically, bumped dies or bumped substrates are required. An overview of the substrate pad metallization and device bumping requirements is listed in **Table 4**.

Especially for flexible substrates, the laser attach brings advantages due to the fact that the interconnection is done immediately and in situ. This is reducing the handling issues of flexible SMD – reflow processes and the associated fixture assembly. In addition common alignment problems of die to flex substrate caused by the thermal extension of the flex during reflow or curing processes are solved by using localized and selective laser heating.

Bumping & Pad Metallization Requirements	
Pad Metal	Al or Cu coated with Ni/Au, Sn, Au
Thin Film	Cr/Au, Ni/Au
Bump	Solder, Ni/Au*, Au*, Solder Cap: e.g. Maskless Meniscus Bump (M2) <i>*electroplated, electroless or stud</i>

Table 4: Bumping Requirements

In order to implement the LaPlace process in the assembly flow of ultra fine pitch LCD drivers (40um – 60um) on Polyimide tape several items have to be addresses:

- 1) a suitable bumping process for ultra fine pitch semiconductor devices has to be selected. In principle the use of standard, established bumping technologies, like electroplated Au bumps is possible, but the use of electroless Ni/Au promises significant

cost advantages due to the absence of photo lithography and masking steps and the high volume wafer production capability in the non-complex electroless process flow.^{6,7,8} However, a ultrafine pitch electroless Ni process has to be qualified and feasibility for LCD drivers must be shown.

- 2) The design of the LAPLACE equipment has to fulfill high die placement and alignment accuracy requirements to meet accuracy specifications of +/-3.5µm or better. On the other hand the tool bond head has to be designed for highest laser heating homogeneity with regard to the large LCD device sizes.
- 3) An overall assembly process has to be established including process flow definition and parameter optimization.

II. Ultra fine pitch bumping

Electroless Ni/Au has already proven its suitability as a low cost bumping process for a broad range of Flip-Chip applications, like Passives, Smart Cards / Smart Labels, ASICs, Memory Devices, etc. With the increasing demand in Flip-Chips and therefore in FC bumping processes, electroless Ni bumps are used as UBM for solder applications, but also as tall stand-off for ACF/NCP assembly.

However, one of the design rules of the standard electroless Ni bumping process describes the limitation in structure size (pad passivation opening) sensitivity at 40um x 40um.⁹ Another important aspect with regard to fine pitch bumping is the Ni bump geometry itself: During Ni deposition, the Ni layer is growing in the same ratio in lateral and in the z- direction once the passivation surface is reached. To overcome these pitch restrictions of the typical mushroom bump shape and structure size limitation the fine pitch capability of the process and minimal structure size sensitivity was be addressed and the established requirements in bump height (electroplated Au bump) for ACF applications was questioned.

By Ni chemistry modification higher pad geometry sensitivity was achieved and the passivation opening size of the LCD devices can now be reduced in order to target smaller bump pitches. Figure 2 shows 10 µm tall Ni bumps on

a LCD driver device. However, plating bath stability decrease on one hand and increase in bump height variation on the other hand were the trade offs of this modification.

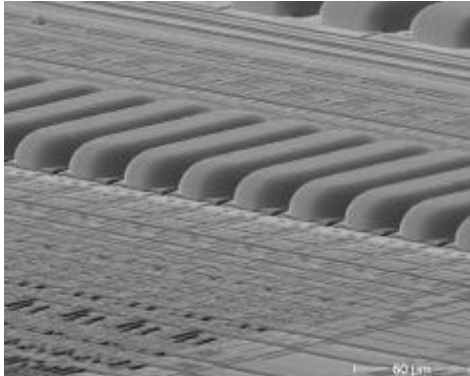


Figure 2: Maskless Meniscus Bump

Therefore, it became necessary to further optimize the Ni plating equipment. New tank materials, indirect bath heating and new techniques for bath circulation are some of the actions, which had been taken. Finally the bath stability was improved and a sufficient bump height distribution within +/- 5 % was achieved.

III. Technical Implementation of LAPLACE for LCD drivers

In order to take advantage of this laser technology for ultra fine pitch LCD driver assembly, PacTech has developed a new Flip Chip Bonder **Figure 4**) in which the laser is integrated in the bond head. The process flow of this new **LAPLACE** process is shown in **Fig 3**.

Integrated in the **LAPLACE** system is a dispense unit which can be used for the dispense of an underfill (e. g., no flow underfill) or a flux for soldering processes.

For adhesive joining processes, dispense of the anisotropic conductive paste or non – conductive paste (NCP) is possible. Prior to dispensing, optionally a preheating stage can be integrated in the tool in order to remove humidity from the substrate and avoid additional voids in the underfill by release of humidity during the Flip Chip attach and curing.

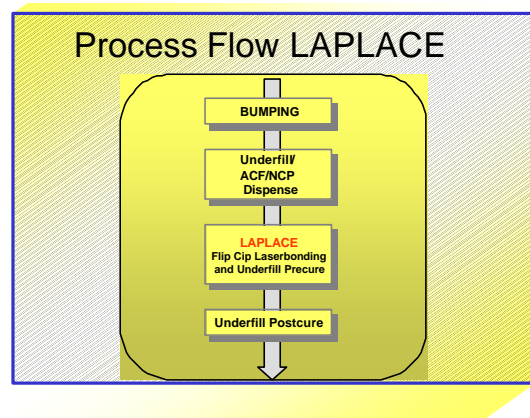


Figure 3: Process Flow LAPLACE

The chips can be picked from waffle packs or from a direct die feeder using the sawing foil. In the bonding tool, which picks the chip by use of vacuum, special laser optics is integrated.



Figure 4: shows a production version of the LAPLACE system with integrated reel – to – reel tool for 35 mm tape and laser class 1 enclosures.

This laser optics is heating the Silicon die from the backside and is inducing the thermal energy into the interconnection to be bonded or into the adhesive by curing it. Thus the laser is used for the soldering process on one side, but also for the curing of the adhesive underfill material or ACF, NCP – material.

Figure 5 shows the bond stage and the camera alignment system of the **LAPLACE** bonder.

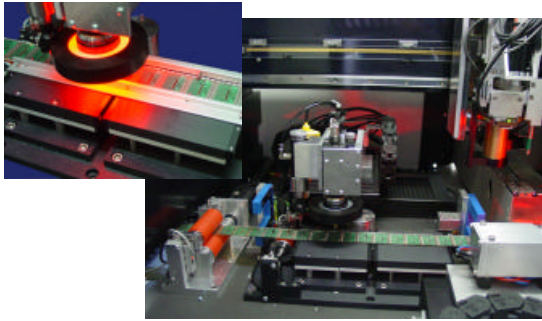


Figure 5: Bond Stage and Camera System of LAPLACE

III Assembly Results

In the following preliminary assembly results on LCD driver applications using ACF and NCP are presented.

Figure 6 shows sample pictures as a process evolutionary overview: The ultra fine pitch LDI (LCD for Drive IC) type device which is already Ni/Au bumped, a top view of the flex substrate before and after assembly of the LDI device in a Chip-on-Flex package (COF).

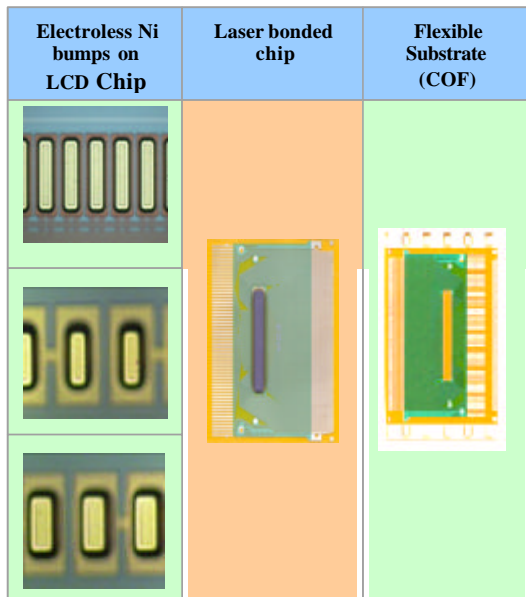


Figure 6: The application of electroless Ni/Au fine pitch bumping for the interconnection between LDI type device and the flexible substrate as COF package, the flexible substrate is made by Samsung Techwin.

To prove the assembly process capability of LAPLACE for anisotropic conductive adhesives, first ACF films were laminated on top of the LDI devices by using separate lamination equipment. Then the chips were placed and assembled by laser heating with the LAPLACE tool. The applied bond force was ~ 18kg. (The maximum bond force possible is 30kg.)

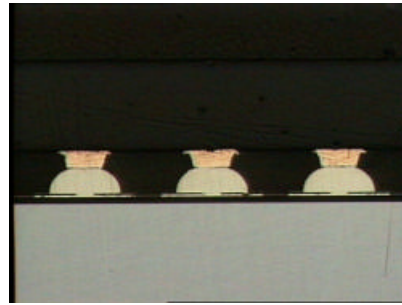


Figure 7 shows the interconnection formed by the conductive particles of compressed ACF material between the Sn plated Copper lead and the electroless Ni/Au bump.

In case of laser assisted assembly using NCP the nature of the interconnection becomes very clear in the cross section shown in **figure 8**: not only the chip was fixed by curing of the NCP also an intermetallic connection between the reflowed Sn coating of the Copper leads and the Au layer of the Ni bumped was formed providing excellent bonding quality and reliability.

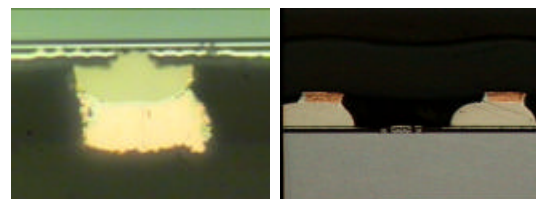


Figure 8: Cross-section of the interconnection between Ni/Au bump and COF package using NCP



Figure 9: NCP - Assembly with LAPLACE

In **figure 9** an overview on a larger interconnection area after NCP assembly is shown. In **table 5** the bond parameter for ACF and NCP assembly are listed.

Since the required Ni/Au bump height for NCP applications is significantly lower than for ACF applications, the ACF material is more expensive compared to the NCP and additional laminate tools are not necessary the assembly using NCP is more cost effective and preferable than the ACF process flow.

Bond Parameter	ACF	NCP
Bond Force [kg]	18	18
Laser Power [mA]	80	80
Pulse Duration [ms]	0.7	1

Table 5: Bond parameters for ACF and NCP assembly of a 2.5mm x 18.5mm chip using LAPLACE.

Beside of ultra fine pitch application a “low precision” version of the laser LAPLACE tool can also be used for the attach of small SMD components, like resistors and capacitors (Figure 10).

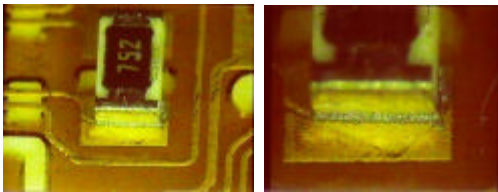


Figure 10: Capacitor Attach using LAPLACE

In flex circuits for many consumer products, the attach of the capacitors and resistors is an issue and requires special fixtures. By use of laser attach, the problem of the fixture is eliminated since the components are fixed and contacted by soldering or adhesive curing directly to the substrate during the short pulse. With regard to LCD driver module assembly usually 10 to 20 passive components have to be attached in addition to the ultra fine pitch driver device. With process cycle times of ~ 1.2 sec/die the LAPLACE process provides a solution for passive or low I/O devices as well. The parts can be pre soldered or placed in printed solder paste depots. Figure 11 shows a proposal of a turnkey solution of a laser assisted assembly line for LCD driver modules.

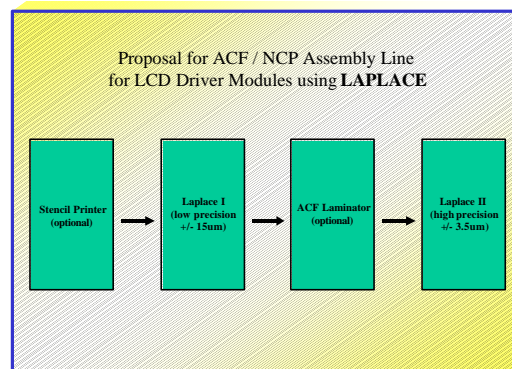


Figure 11: Laser assisted assembly line for ultra fine pitch & low I/O count devices

IV Summary

A new bonding method using a laser heated tool integrated in a FC bonder was developed. The advantages of laser physics have been discussed and demonstrated.

The new process and tool concept is suitable for applications based on smart cards on flexible circuits, LCD drivers and high end flexible circuits, but also die attach on ridged substrate. In principle, LAPLACE is compatible with all types of Flip Chip interconnections which are state-of-the-art in industry today, but especially on ultra fine pitch devices the flexibility and accuracy of the system were perfectly demonstrated. ACF or NCP based assembly processes for ultra fine pitch and solder based low I/O count device attach were conducted by using the new laser based technology. The process capability of cost reduction together with low cost bumping methods like electroless Ni/Au was shown.

References

- /1/ L. F. Miller, "Controlled Collapse After Reflow Chip Joining", IBM J. Res. Develop., Vol. 13, pp. 239-250, May, 1969.
- /2/ P. Kasulke, W. Schmidt, L. Titerle, H. Bohnaker, T. Oppert, E. Zakel, "Solder Ball Bumper SB²-A flexible manufacturing tool for 3-dimensional sensor and microsystem packages", Proceedings of the International Electronics Manufacturing Technology Symposium (22nd IEMT), Berlin, April 27-29, 1998
- /3/ G. Azdasht, L. Titerle, H. Bohnaker, P. Kasulke, E. Zakel, "Ball Bumping for Wafer Level CSP - Yield Study of Laser Reflow and IR-Oven Reflow", Proceedings of the Chip Scale International, San Jose CA, September 14-15, 1999
- /4/ Elke Zakel, Lars Titerle, Thomas Oppert, Ronald G. Blankenhorn, "High Speed Laser Solder Jetting Technology for Optoelectronics and MEMS Packaging", Proceedings of the International Conference on Electronics Packaging (Tokyo, Japan), Apr. 17-19, 2002
- /5/ De Haven, Dietz, "Controlled Collapse Chip Carrier (C4) an Enabling Technology", Proceedings of the 1994 Electronic Components and Technology Conference (44th ECTC), Washington D.C., pp. 1-6. 1994.
- /6/ T. Teutsch, T. Oppert, E. Zakel, D. Tovar, "A Bumping Process for 12 Wafers", Proceedings of the IEMT Symposium (24th IEMT), Austin TX, pp. 328-333, October 18-19, 1999
- /7/ T. Teutsch, T. Oppert, E. Zakel, "A Roadmap to Low Cost Flip Chip and Proceedings of the International Electronics CSP using Electroless Ni/Au", Manufacturing Technology Symposium (IEMT) Symposium, Omiya, Japan, April 15-17, 1998
- /8/ T. Teutsch, T. Oppert, E. Zakel, D. Tovar "A Bumping Process for 300 mm Wafers", Proceedings of the HDI Conference, Phoenix AZ, September 25-27, 2000
- /9/ Pac Tech Webpage: www.pactech.de