

Low Cost Wafer Bumping for Power Electronics Device Interconnection

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Abstract

Within the last years electroless Ni/Au has developed, especially for cost driven applications, e.g. RFID, Memories, protection devices, to an established low cost wafer bumping technique. Beside cost aspects also performance requirements make the use of electroless Ni/Au UBM very attractive to the electronic and packaging industry. High end applications are addressing challenging requirements with regard to environmental (high temperature) or electrical (high power) aspects and are moving step by step towards this emerging technology.

This paper will discuss the application of electroless Ni/Au as a solderable interface for power switch devices using two different different interconnection techniques:

The large area contacts (source and gate) of high power IGBT transistors were plated with Ni/Au to enable solder connection during assembly. Ni film thickness and stress behavior were optimized to meet the technical specification and to provide a reliable and suitable Ni layer metallurgy.

For a similar application the glass passivation on top of the transistor contacts of a MosFET device (PowerMOS) have been patterned in an area pad opening configuration to enable Flip-Chip assembly and to achieve better power and thermal management properties. Fine pitch solder stencil printing was performed on the Ni/Au UBM bumped Flip-Chip contacts. Reliability data for the assembled Flip-Chips is presented and discussed.