

# Lead Free Solder Bumping for Flip Chip and Wafer Level CSP

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## Abstract

The implementation of lead free processes on wafer level has special requirements due to the technologies used in the wafer level bumping processes.

This paper will give an overview of interconnection technologies in combination with flip chip. On one side, the technical solutions regarding polymeric and adhesive attaches are presented. All the solutions are representing lead free technologies which are in use today and are being implemented in volume products.

On the other hand, the technical challenge for bumping is the formation of lead free solder bumps.

The paper presents an overview of the solder bumping technologies used today:

1. Electroplating of solder
2. Wafer level stencil printing using solder paste
3. Wafer level solder ball transfer and solder ball reflow

The technological solutions for lead free solder are having certain limitation. Especially, electroplating process is technically limited to SnAg alloys.

An overview of the solder alloy compositions in SnAg which are in evaluation today will be given.

Wafer level stencil printing is allowing a larger flexibility for the selection of lead free solder alloys. The materials qualified today are based on SnAg and SnAgCu. The results with qualification of these alloys in reliability tests is presented.

The last technology of solder ball transfer and reflow is providing the largest flexibility for solder alloy selection. The results of qualification for different solder alloys is presented.

Finally, a comparison of the three technologies – electroplating, wafer level stencil printing and wafer level ball placement is given.