

A Performance Driven Bumping Solution for Automotive Power Electronics

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Abstract

Within the last years electroless Ni/Au has developed to an established wafer bumping technique supporting advanced Flip-Chip assembly technology. Hereby electroless Ni/Au, as an Under Bump Metallization (UBM), combined with wafer level solder stencil printing or solder ball placement provides outstanding advantages, especially for cost driven applications, such as RFID, Memories and protection devices.

Beside of cost aspects also performance requirements make the use of electroless Ni/Au UBM and mass production capable soldering processes very attractive to the electronic and packaging industry. One example is the high power version of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

The lower power MOSFET devices are already implementing low cost bumping techniques to provide wafer level CSP packages - mainly driven by cost aspects. In comparison, the attraction for high end applications in the use of these bumping techniques is based in the very low electrical resistance of the FC interconnection, excellent thermal dissipation (when combined with thermal boards), high reliability, multilayer interconnect capability and small package size.

This paper will discuss the implementation of electroless Ni/Au and wafer level stencil printing of eutectic SnPb37 solder for Flip Chip packaging for automotive power electronics.

To enable Flip-Chip assembly on a high thermal performance power MCM substrate the wafer glass passivation on top of the transistor contacts (source, gate) of a power MosFET device (2-4 W) has been patterned in an area array pad opening configuration. Fine pitch solder stencil printing (300-350um) was performed on the Ni/Au UBM bumped Flip-Chip contacts. Reliability data achieved after Flip-Chip assembly and underfill application is presented and discussed.

