Low Cost Wafer Bumping of GaAs Wafers

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Abstract

The microelectronics industry has implemented a significant number of process technologies to accomplish the various packaging and backend operations. These technologies have been successfully implemented at a number of contract manufacturing companies and also licensed to many of the semiconductor manufacturers and foundries. The largest production volumes for these technologies are for silicon based semiconductors which are based on either aluminum or copper interconnect metallurgy. The direct transfer of these technologies to compound semiconductor devices, like GaAs, LiTaO3, and GaN, is limited due to a number of technical compatibility issues and several perceived compatibility issues [1-4].

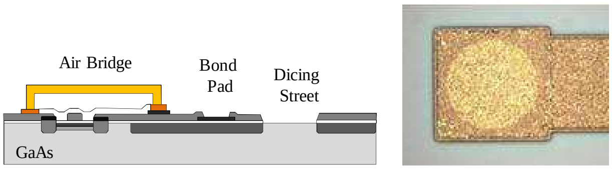
From a technical standpoint, many of these high end devices contain fragile air bridges, gold bond pads, cavities & trenches, and unique bulk material properties which are sensitive to many of the mechanical and chemical processes associated with many of the standard packaging operations using for silicon wafers. Special care must be taken to ensure that there is no mechanical stress put on the wafer during any of the handling operations associated with deposition of the UBM, solder bumping, wafer thinning, dicing, and die sort. In addition, many chemicals used for resist stripping, metal etching, and solder fluxing will react with some of the materials on these compound semiconductor devices.

From a perception standpoint, companies which are processing large numbers of silicon based semiconductor wafers in their packaging and backend facilities, are reluctant to process many of these compound semiconductors because there is a perceived issue with cross contamination between the different wafer materials. Companies are not willing to risk their current business of processing silicon wafers by introducing these new materials into their existing process flow.

The strategy in this study is to protect all structures and surfaces with a resist or film as part of each step in the process. This protects the wafer from mechanical and chemical damage; and at the same time protects sensitive fab processes from contamination by the compound semiconductor.

Introduction

The test vehicle for this program is a GaAs device which contains both air-bridges and has gold bond pads. If solder were deposited directly onto the gold bond pads, the gold would be partially consumed during the solder reflow process, and will eventually fail in the field due to thermal and electro-migration processes. An under-bump-metallization (UBM) is required to keep these destructive processes form occurring.



Schematic drawing of GaAs test vehicle and an optical image of a gold bond pad on the device.

Experimental

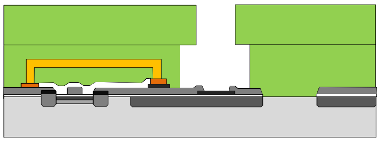
There are several options for depositing the UBM on the wafer, including: sputtering, electroplating, or electroless plating. None of these are directly transferable to GaAs devices. For example, the use of a thin film sputtering process, followed by subtractive etching of the metal layers, requires that all surfaces of the wafer be coated with metal and then selectively etched with either caustic or acidic chemicals. There are number of opportunities for degradation of both the air bridges and various semiconducting materials using the sputtering method.

One will encounter many of these same interactions which can damage or destroy the GaAs device by using electroplating technologies to form the UBM. The electroless nickel/gold plating process (ENIG), unfortunately, will not initiate on the gold bond pads, and therefore it is also not directly compatible with GaAs devices with gold bond pads.

In this study, a combination of resist deposition, thin film sputtering, and electroless nickel/gold technologies were used to create the UBM.

To convert the gold surface of the bond pad over to a metal which is compatible with the electroless nickel/gold process, thin layers of titanium and copper were sputtered onto the GaAs wafer using a liftoff process. The use of a liftoff process has the advantage over a subtractive etch process, in that the liftoff resist protects the whole wafer form chemicals and mechanical damage [5].

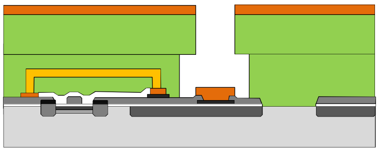
A standard positive resist was coated onto the wafer using standard spin coating equipment, soft baked on a hot plate, and flood exposed. This layer was approximately 3-4µm in thickness. A second layer of resist was coated on top of the first resist layer using a slower spin speed to create a thicker layer on top of the first (~5-6µm). This layer was then pattern exposed and batch developed to open up the area above the bond pad. By controlling the develop time, the bottom layer which was flood exposed, will also be developed to create a slightly larger diameter opening in the resist layer closest to the wafer.



Step 1. Deposit and pattern a dual layer liftoff resist.

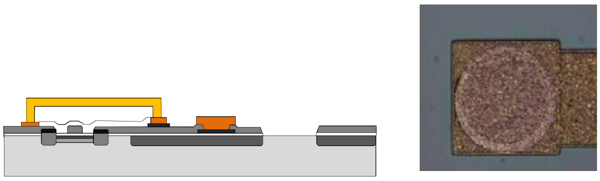
The resist stack was then baked to make it stable to the subsequent sputtering process. All films baked in the range of 100 ºC to 200 ºC were found to be stable to the sputtering process.

The sputtering of Ti and Cu was accomplished using a standard magnetron sputtering tool that was capable of RF pre-sputtering the wafer with argon and was also equipped with a chilled wafer platen [6]. After Ar pre-cleaning, 500 Å of Ti was deposited on top of the gold to create an adhesion layer and diffusion barrier. A 6000 Å layer of copper was then sputtered on top of the Ti layer. The thickness of this Cu layer must be thick enough to be stable in the subsequent electroless plating steps and thin enough not to create a metal bridge between the liftoff resist layers.



Step 2. Sputter deposit 500 Å of Ti followed by 6000 Å of Cu.

The films baked at 100 ºC were found to be easily stripped after sputtering using either acetone or NMP at room temperature. Films baked at higher temperatures took longer to strip or required elevated temperatures to strip.

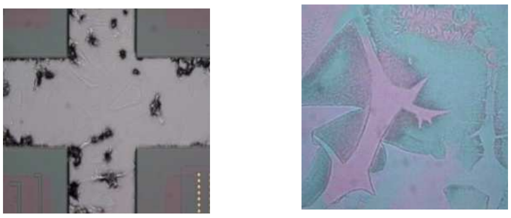


Step 3. Strip the liftoff resist from the wafer.

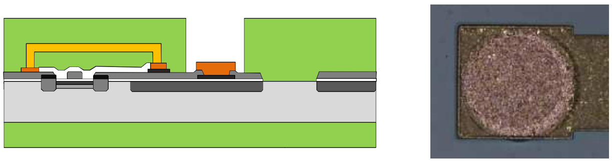
The electroless nickel and gold plating process is often described in the literature as selective. This is true for most silicon wafers where the all structures are protected by a silicon nitride passivation. GaAs devices have many exposed metals and doped areas where nickel will plate. These areas need to be protected by a material which is easily applied, can survive the aggressive chemistries in the plating line, and be easily removed; all without damaging the air bridges or exposed materials on the wafer.

Examples of spurious Ni/Au plating in the scribe streets and on air bridges of an unprotected GaAs device.

A large number of resists were evaluated for the top side protection coating. Only one was found to survive the electroless nickel process and still be easily removed in an inert solvent. All of the novalac based resists that we evaluated required a very hard bake at ~200 °C in order to survive the electroless plating process. Removal of this resist requires very harsh chemicals or alternatively plasma ashing, which both damage the wafer.



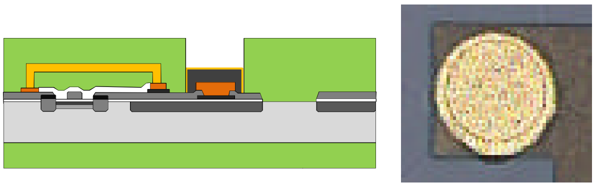
Examples of damage to the GaAs wafer using piranha etch chemicals and plasma ashing to strip the resist.



Steps 4-5. Deposit and pattern a protective resist on the frontside and then laminate a UV release film on the backside of the wafer/

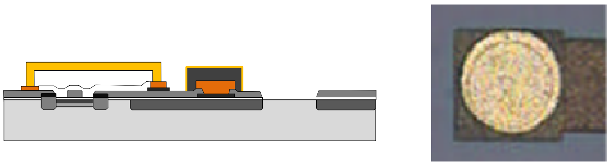
A UV release film was laminated onto the backside of the wafer to protect the backside from spurious plating which is often initiated on bare GaAs.

The electroless nickel/gold plating process is carried out using an automated plating line which sequentially processes the wafers through a series of chemical baths and rinse stations [7-8]. The first bath in the plating sequence is a dilute acid used to clean the pads of any residual organic or silicon based contaminates. The second step is to remove any native oxide that may have built up on the copper pad surface. This is performed using a much stronger acidic solution. This solution also etches some of the copper. The next step is to activate the surface of the copper using a palladium catalyst. This is followed by immersion in a nickel sulfate based plating bath and then an immersion gold plating bath. A nickel height of 3 microns and a 500Å layer of gold were deposited in this study



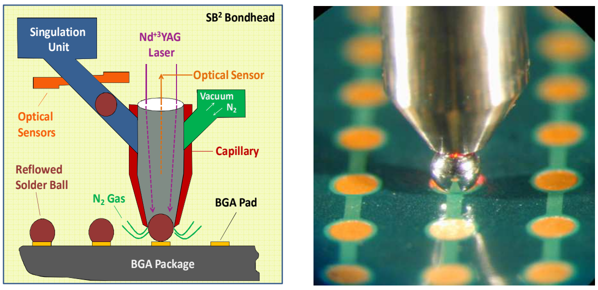
Step 6. Electroless Plate 3 μm Ni and 500 Å Gold

The laminate film on the backside of the wafer was removed by first exposing the film to UV light and then peeling off the film. The thin film resist on the frontside was removed by immersion in a solvent at 65ºC. Several prebake conditions were also evaluated for this protective resist. If the baking temperature was kept below 150ºC, the resist was easily removed without affecting the GaAs wafer.

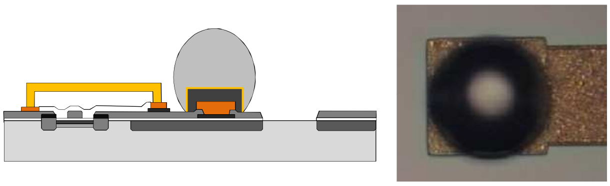


Steps 7-8. Expose and remove backside laminate film, and strip the frontside resist.

Some of the same concerns about mechanical and chemical degradation during UBM deposition are also relevant to the operations related to solder bumping. Several options exist for solder bumping, including: paste printing, electroplating, or sphere placements [9]. Each of these technologies would require a unique set of resists to protect the GaAs structures from damage during processing. In this study, a laser based bumping process which drops a single solder sphere onto the bond pad and then laser reflows the solder just as it reaches the pad was used [10-12]. This process has no mechanical contact with the wafer and is fluxless, thus eliminating any chemical interactions with the device or need for protective resists. Solder bumps are deposited at a rate of 6-10 spheres per second.

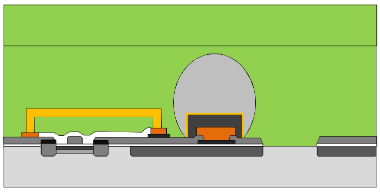


Schematic diagram of the solder bumping tool and a picture of the tool dispensing a solder bump.



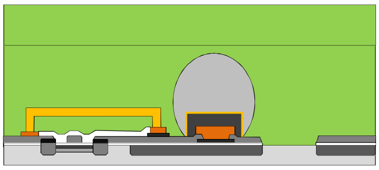
Step 9. Solder bump using laser based sphere jetting system.

After bumping, many device designs require the wafer to be thinned before singulation. The grinding process in inherently mechanical in nature and special care must be used to protect the frontside of the wafer. In this study, a spin on resist was deposited onto the front surface of the wafer followed by lamination of a UV release tape on top of the resist.



Steps 10-11. Spin on blanket layer of resist on to the frontside of wafer and laminate a UV release film on top of the resist.

The wafers were then ground using a standard grinding tool equipped with a polygrind option.



Step 12. Grind and polish

One measure of thinning quality is the ability to repeatedly grind wafers to the same thickness. The following chart shows the thickness distribution of 600µm GaAs wafers which were ground to a target thickness of 300µm, with a tolerance spec of ±12µm.

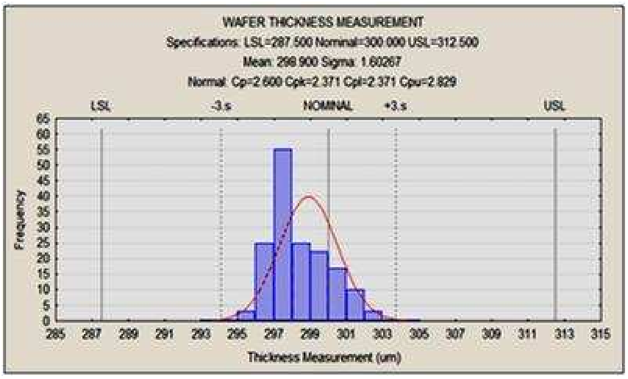
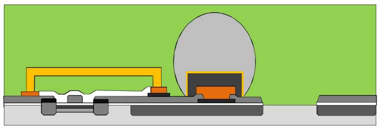
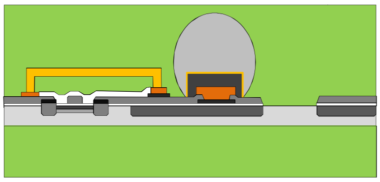


Chart showing the thickness distribution of ground wafers.

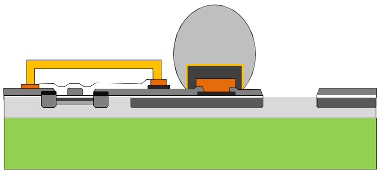
After thinning, the laminate film is removed from the frontside of the wafer and another UV release film (dicing tape) is laminated onto the backside. The spin on resist on the frontside is then removed.



Step 13. Expose and remove laminate from frontside

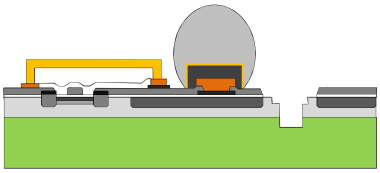


Step 14. Laminate dicing tape onto backside

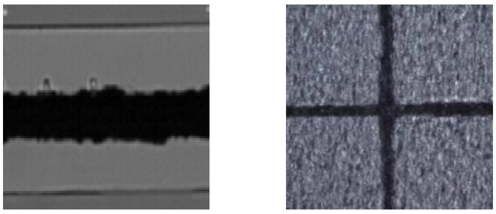


Step 15. Strip resist from frontside

Dicing is performed using a dual spindle tool and two different blade widths.

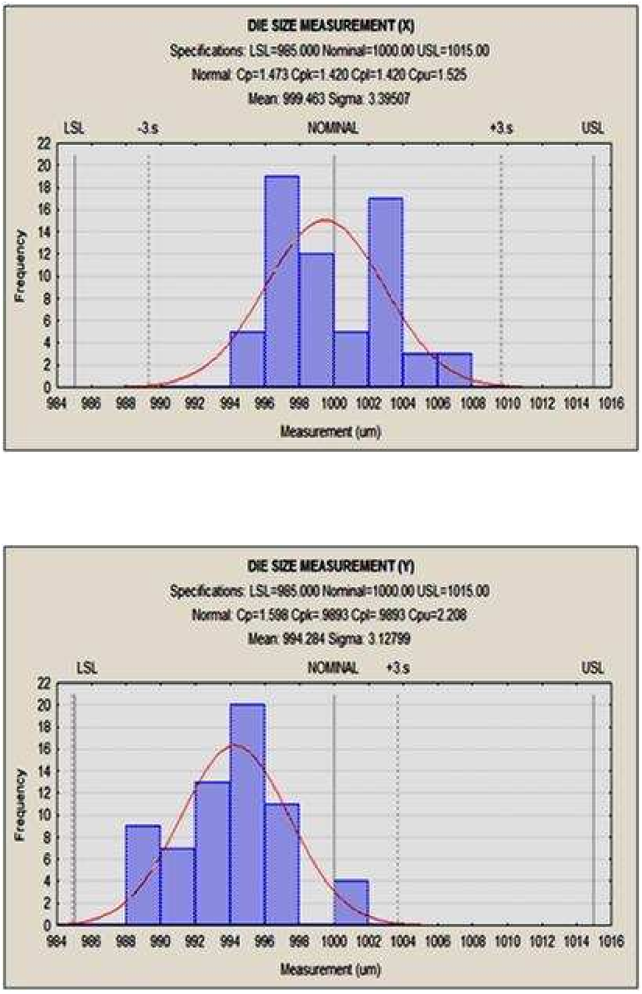


Step16. Dice wafer using two step cut



Optical images of the dicing quality on the front and backside of the GaAs wafer.

One measure of the dicing quality is the ability to repeatedly dice the die to the same size. The following chart shows the die size distribution where the target die size was 1000µm square, with a tolerance spec of ±20µm.



Charts showing the die size distribution in the x and y dimensions.

The final backend operations in the process flow are to pick the good die off the dicing tape and placed into the tape and reel pockets.

Conclusions

A set of packaging and backend operations were developed to process GaAs wafers though: UBM, solder bump, thin, and dice. The strategy of using a set of resists and laminate films to protect the wafer from both chemical and mechanical damage enabled the use of several common technologies to process the wafers.

Acknowledgements

The authors would like to thank all the engineer and technicians at PacTech for their contributions to this project.

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