Wafer Level CSP using Low Cost Electroless Redistribution Layer

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A LOW COST ELECTROLESS PROCESS FOR WAFER LEVEL CSP AND RDL

Modern microelectronic products requires miniaturized packages, like Flip Chip and CSP. Besides the driving force of miniaturization and reduction in size and weight, the main advantages of flip chip and CSP for modern portable telephone communication products is their increased performance at high frequencies. Flip chip and direct attach of chips on the board offers straight forward solution for miniaturization.

A key requirement for flip chip is bumped wafer. For bumping several technical solutions are available, like evaporation, electroplating and electroless bumping. Electroless bumping offers the most elegant and lowest cost solution. For an optimal implementation flip chip technology design of the IC pad configuration in an area configuration is required if the number of IO’s is increasing and the pitches are becoming smaller and smaller. However, we must state that the key for flip chip is not only ultra fine pitch bumping in a pitch below to 200 µm going to 100 µm and lower. The key for flip chip in ultra fine applications is, especially, the availability of printed circuit boards in a pitch below to 200 µm.

Most wafers today are designed for wire bonding with peripheral pad configurations in ultra fine pitch. These are not ideal solutions for flip chip, due to the reasons mentioned before. In order to overcome this problem, an interim solution is wafer level redistribution of the pads from peripheral to area array pads with larger sizes and a relaxed pitch.

This paper describes a low cost electroless Ni/Au Under Bump Metallization (UBM) and a wafer level redistribution process based on electroless copper circuitization. It includes the use of a novel plasma enhanced chemical vapour deposition (PECVD) process to deposit a bifunctional nano-layer acting as an adhesion promotor and as a catalyst for electroless copper deposition. The described techniques are suitable for all wafer passivation types, which are used in industry today. The complete redistribution process is based on batch processing and less masking and photoimaging steps. By using the electroless Nickel process and wafer level stencil solder printing the process is highly cost efficient and has large volume manufacturing capability.
Introduction

A standard technology for a wafer redistribution process is based on sputtering and high end dielectric technology, like BCB (Benzo Cyclo Buthen) or PI (Polyimide). This process is associated with high cost. On the other hand, a process which avoids sputtering technology is able to major cost savings for wafer level redistribution.

This paper presents semi – additive approach to wafer level redistribution:

In a first step, the bond pads on the wafer are passivated using electroless Nickel/ Gold. The process steps for electroless Nickel/ Gold are well – known in industry.

PacTech has developed a process for electroless Nickel/ Gold UBM which is now implemented in a high volume production line – PacLine 2000 [3].

Fig. 1: Automatic Electroless Nickel/Au Bumping Line

The process uses wet chemical dipping procedures in well controlled chemicals and environment avoiding sputtering and photo – imaging steps. In the second step, dielectric in a thickness of 5 – 10 µm, optionally 15 µm, is applied on the wafer level.

This dielectric is, ideally, a photo – imaginable material. After photo – imaging, the diameter is opened in the area above the bond pads which are prior protected with electroless Ni/ Au bumps.

In the next steps the dielectric is prepared with a special catalytic material which provides, besides its catalytic properties, an optimum adhesion to the subsequent electroless copper plating. Electroless copper plating is done in batch processing of 25 to 50 wafers. The advantage of using electroless copper plating over electroplating is the possibility of batch processing. This allows an extremely high throughput and reduction of process cost. The electroless copper can be deposited in its full thickness, up to 5 µm, with a special high speed copper bass. After plating to the desired and required thickness which is, ideally, 5 µm on the full wafer scale, the electroless copper film is etched after applying a second photo – imaging step.

Fig. 2: Wafers in parallel Ni/Au batch processing

Finally, before electroless Ni/ Au can be applied either on the full wafer level or, selectively, in the pad areas of the redistribution structure. For a wafer level redistribution, respectively wafer level CSP, an additional solder mask is applied by a second layer of dielectric. The dielectric is photo – imaged in a third process step and opened in the area above the solder bumps which will be attached to the printed circuit board. A final step for the wafer level redistribution is the application of an additional solid state bump. This solid state bump can be electroless Ni/ Au as bump. The electroless Ni/ Au bump on the redistribution wafer is, ideally, suited for ACF or conductive adhesive joining.

Alternatively for soldering processes, solder spheres are required. In order to improve the reliability and thermal fatigue resistance of the redistributed flip chip layout, solder spheres with a large diameter are preferred. 300 µm diameter solder spheres in a pitch of 500 µm cannot be applied with wafer level stencil printing. Wafer level stencil printing is limited to larger pitches if 300 µm diameter solder spheres are required. For 500 µm pitch wafer level ball placement and reflow is the preferred process.
Electroless Nickel is used in industry for a wide range of applications in which Al work pieces are plated with Ni. The equipment available for these standard processes based on large work pieces or printed circuit boards is not suitable for wafer bumping. In order to fulfill the specific requirements for wafer bumping a new modular electroless Ni wafer bumping line has been developed. Each module can take batches of 50 wafers 8” or 10 wafers 12”. Such processing is a key to the extremely high throughput of this bumping line which again determines the overall cost of the bumping process.

Before the wafers can be metallized in the line the wafer backside has to be covered by a stable resist prior to the chemical bumping process. The next step is a treatment of the pads in an Al cleaner which removes oxide layers while the Al surface is micro-etched. The pretreatment is done in the first modules of the line. An alkaline zincate solution is used for activating the Al surface. For the electroless Ni plating a bath based on sodium hypophosphite is used. The rate of Ni deposition is 20µm/h. A final Au coating on the Ni is necessary to prevent oxidation and enables long-time solderability of bumps. With this Au coating a maximum Au thickness of 0.25µm can be achieved (typ. 0.05µm). The complete process flow is shown in figure 5. The quality of bumps is controlled by optical microscopy, profilometer...
measurements and shear tests. For detailed analysis cross-sectioning, SEM and EDX are used.

**Fig. 5: Ultra fine pitch bumping (Pitch: 50µm)**

The minimal bump height is 1µm to have a closed and voidless Ni-Layer. The maximal height is limited by the pad to pad spacing. The bump height must not be larger than ½ pad spacing minus 5µm to avoid short circuits between neighboring pads by over-growing Ni. A height of 5µm is recommended for FC soldering. Figure 6 shows a part of an electroless Ni/Au bumped Wafer with a pad pitch of 50µm. This meets the requirements of reliability and fast processing. The adhesion of the bumps on the Al pads depends on the pad area. For 100 x 100 µm pads the shear strength is at least 100g.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Acceptable Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer size</td>
<td>4” (100 mm) – 12” (300 mm)</td>
</tr>
<tr>
<td>Wafer backside</td>
<td>Any</td>
</tr>
<tr>
<td>Pad geometry</td>
<td>Any (square, rectangular, round)</td>
</tr>
<tr>
<td>Pad size</td>
<td>&gt; 40 µm for production (&gt;10 µm for prototyping)</td>
</tr>
<tr>
<td>Pad spacing</td>
<td>≥ 2x bump height + 10µm for production (&gt;5 µm for prototyping)</td>
</tr>
<tr>
<td>Metallization</td>
<td>AlSi 1%, AlSi 1% Cu 0.5% or AlCu 2%</td>
</tr>
<tr>
<td>Al thickness</td>
<td>1 µm for production (0.5 µm for prototyping)</td>
</tr>
<tr>
<td>Wafer probing</td>
<td>Before or after Ni/Au plating</td>
</tr>
<tr>
<td>Passivation</td>
<td>Defect-free nitride, oxide, polyamide, without any residues on the pads</td>
</tr>
<tr>
<td>scribeline</td>
<td>Isolated (test pads acceptable)</td>
</tr>
</tbody>
</table>

**Tab. 1: Characteristics of Ni/Au Bumps**

<table>
<thead>
<tr>
<th>Bump characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Recommended height for FC Soldering</td>
<td>5 µm</td>
</tr>
<tr>
<td>Maximum height</td>
<td>≤½ pad spacing -5µm</td>
</tr>
<tr>
<td>Material</td>
<td>NiP 10%</td>
</tr>
<tr>
<td>Resistivity</td>
<td>70 µΩcm</td>
</tr>
<tr>
<td>Hardness</td>
<td>550 mHV</td>
</tr>
<tr>
<td>Adhesion to Al 100x100 µm² pad</td>
<td>&gt;100g (typ.150g)</td>
</tr>
<tr>
<td>Au coating thickness</td>
<td>0.05 – 0.25 µm</td>
</tr>
</tbody>
</table>

**Tab. 2: Design rules for the Ni/Au bumping process**

For achieving reliable and reproducible results regarding the electroless Ni/Au bumping of several types of wafers from 4” up to 12”, design rules have been defined. As pad materials AlSi 1%, AlSi 1% Cu 0.5%, AlCu 2% and other alloys of these metals were investigated. All types have been processed with good results. Nevertheless there are some restrictions on the wafers to be Ni bumped. The Al bondpad thickness should be 1µm or more in order to have sufficient Al after cleaning and activation. There are no limits to passivation thickness but the passivation must be free of defects. Cracks cause a growth of Ni which can produce short circuit. This will also occur on parts of a wafer surface which were scratched by improper handling. Ni also grows on Si which is not covered by an oxide or passivation layer. Unprotected Si in the wafer scribe line will cause plating of a Ni layer with low adhesion. Therefore the scribe line should be almost insulated, except for defined process control structures. A summary of the wafer design rules is shown in table 2 [7].

All these results and requirements can be transferred to electroless Ni/Au bumping on Cu pads. Of course the Ni/Au process has to be modified, especially the pretreatment and activation processes have to be changed for bumping on an other bond pad metallurgy.
The new electroless Ni/Au on Cu process will be qualified together with the redistribution process within the next few months by doing the necessary reliability investigations.

**Wafer Level Redistribution – “ElastoPAC”**

To start with the wafer level redistribution a redistribution design has to be made first.

As an example and a test vehicle Pac Tech’s 4 inch test wafer Pac2.1 with a peripheral layout of 200 micron pitch and a PSG passivation was used. Figure 7 shows the redistribution design for the Pac 2.1 test wafer.

![Fig. 6: Redistribution Layout for Pac 2.1 Test Wafer](image)

Tab. 3: Characteristics of Photodielectric

<table>
<thead>
<tr>
<th>Dielectric characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material</td>
<td>Epoxy based</td>
</tr>
<tr>
<td>Thickness</td>
<td>10 µm</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>1 MHz: 4.1</td>
</tr>
<tr>
<td></td>
<td>1 GHz: 3.4</td>
</tr>
<tr>
<td>Insulating Resistance</td>
<td>$10^{14} , \Omega$</td>
</tr>
<tr>
<td>CTE</td>
<td>60 - 70 ppm/°C</td>
</tr>
<tr>
<td>$T_G$</td>
<td>130 - 150°C</td>
</tr>
<tr>
<td>Water Absorption</td>
<td>&lt; 0.5%</td>
</tr>
</tbody>
</table>

![Fig. 7: Process flow for Wafer Level Redistribution (Photomasking steps in red)](image)

Initially the redistribution starts with Ni/Au bumping of the Al bond pads up to an Ni height of 5 µm (Fig. 8). Then a epoxy based dielectric is spun on the existing wafer passivation. The mechanical and electrical properties of the dielectric are listed in table 3.

![Fig. 8: Cross section of wafer level redistribution](image)

Wafer passivation material can be SiN, SiO$_2$, PSG as well as PI. Additionally to our standard dielectric BSC and PI is currently under evaluation.

For full area copper deposition a seed layer formation will be followed by an electroless Cu plating batch process. There are two prerequisites of electroless copper metallization of a dielectric material. First, adhesion must be obtained and second, proper catalytic activation has to be achieved.
The seed layer generation takes place as a gas phase plasma process (PECVD). Therefore, a plasma reactor with a parallel plate design and a RF-powered circular substrate electrode is used. This process is developed by Atotech for direct metallization of dielectrics for future requirements in PCB industry [6] and specially adapted for wafer applications. Figure 10 shows a scheme of the PECVD chamber and gives the standard plasma parameters.

![Fig. 9: Scheme of the PECVD chamber](image)

The plasma metallization consists of three different steps. In a first pretreatment step the dielectric is conditioned by plasma without roughening the surface in contrast to wet chemical processes. The second step is the deposition of a 5 - 10 nm thick transition metal layer by PECVD. In a subsequent third step, this catalytically active seed layer activates an electroless copper metallization bath.

This direct metallization by PECVD is applicable to a wide range of polymers which are used as dielectric in electronic industry like PI, epoxy resins or even fluoro polymers for high-frequency applications. It leads to very strong polymer-metal adhesion without roughening of the polymer surface. E. g. on PI adhesion of more than 20 N/cm (peel off test) is reachable.

The Cu becomes structured by an photomasking and etching process. At least the surface is covered by an solder mask and the opened Cu bond pads are NiAu bumped again.

The results of the Cu redistribution Layer for our test vehicle is shown in figure 11.

![Fig. 10: Cu Redistribution Layer](image)

Solder bump formation can be done by solder stencil printing, where an automatic printing machine is used.

Typical solder paste are Pb37Sn63 alloys with particle sizes below 20 µm. The stencil apertures are adapted to the specific application. The volume of the printed paste is determined by the aperture diameter and stencil thickness. The selection of appropriate stencil geometry is essential for printing with high yield. Special design rules have been developed for this process [7]. The subsequential solder is reflowed and flux residues are cleaned. The solder volume after reflow will be approx. 50% of the paste volume. Figure 12 shows printed solder paste after reflow in a pitch of 180 µm.

![Fig. 11: Stencil printed Solder Bumps](image)

Figure 9 shows a detailed cross section drawing of the complete redistribution layers.

**Wafer Level CSP – “ElastoPAC”**

To implement the wafer level redistribution into a wafer level CSP it is necessary to increase the solder bump height. Pac Tech is using a propriety process, which cannot be shown in detail at the moment. Essentially it is necessary to use techniques like LS² and SB² for solder ball attach [8,9].

The LS² process, like it is shown in figure 13, combines 2 techniques:
1) solder ball gang placement by using a stencil
2) solder ball reflow by using a laser scanner
The advantages due to stencil printing are, the possibility to apply a higher solder volume on the redistributed pads and the much easier and more efficient flux cleaning compared to an oven reflow, because of the only locally applied laser energy, which will not effect the flux residues beneath the solder spheres. An additional advantage of a ElastoPAC as a wafer level CSP is that for encapsulation halogen-free components can be use.

The SB$^2$ is used for repair of sites with missing or bridged balls.

Solder application can be done by stencil printing and in the case of an wafer level CSP by LS$^2$ method.

In the near future reliability data on all of the presented new techniques will be available:
- Redistribution of 2 sensor devices followed by assembly and thermal cycling investigations are under preparation and will be available in Q2/2000
- Ni/Au on Cu is already available for prototyping services and will be qualified on customer products soon

References

Fig. 12: LS$^2$ – Ball Gang Placement and Laser Reflow [9]

Summary and Outlook
A new low cost wafer level redistribution process was presented. Using eletroless Ni as a key technology the process fulfills together with other wet chemical batch plating techniques, like electroless Cu, and the less masking steps the requirements of a low cost process.

Further advantages of electroless Ni are the selective plating on Al and Cu bond pads and the ultra fine pitch capability.

The epoxy based photodielectric makes the process capable for all wafer passivation types, which are used in industry today and offers as a plating base a reliable adhesion for the Cu redistributed bond pads and circuits. The PECVD deposition of the seed layer for electroless Cu plating opens due to the flexibility of the process beside high adhesion also perspectives for the metallization of future polymer dielectrics.