Low Cost Flip Chip Bumping

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Abstract

A driving force to achieve increased speed and performance along with higher I/O count is the Flip Chip (FC) Technology which has therefore an high level of importance for a variety of applications. A breakthrough, however, will be the use of flip chip due to cost reduction. For this aim it is essential to use low cost bumping techniques.

However, to provide FC technologies also for devices with high I/O count and high pin density applications like Microcontrollers, RAMBUS devices, etc.... it is necessary to redistribute the historically peripheral bond pads with ultra fine pad pitch into a wafer level CSP.

This paper describes a low cost electroless Ni/Au Under Bump Metallization (UBM), a wafer level redistribution process based on electroless copper circuitization and different methods of single and multiple solder ball placement.

Electroless Ni/Au Bumping

The electroless Ni/Au bumping is a wet-chemical and maskless process. With the developed manufacturing process all types of wafers can be bumped with a standard process in excellent quality. In a special designed bumping line wafers, from 4” (100 mm) to 12” (300 mm) diameter can be plated [3,7].

The key for a successful, reproducible and reliable manufacturing process is in the used chemicals and equipment. The electroless Nickel bumping process can be performed with standard chemicals available on the market for simple test structures and test dies without electrical inner circuitry. However, when applied to functional wafers with complex inner electrical structures, different metallization and different passivations, the process requires specific proprietary chemical compositions and know how for a reproducible and reliable result. Here is the key to electroless Nickel implementation in production.

This is an explanation for the multitude of investigations and research projects in industry and in institutes which did not lead to a direct manufacturing process in the past.

Electroless Nickel is used in industry for a wide range of applications in which Al work pieces are plated with Ni. The equipment available for these standard processes based on large work pieces or printed circuit boards is not suitable for wafer bumping. In order to fulfill the specific requirements for wafer bumping a new modular electroless Ni wafer bumping line has been developed. Each module can take batches of 50 wafers 8” or 10 wafers 12”. Such processing is a key to the extremely high throughput of this bumping line which again determines the overall cost of the bumping process.
Before the wafers can be metallized in the line the wafer backside has to be covered by a stable resist prior to the chemical bumping process. The next step is a treatment of the pads in an Al cleaner which removes oxide layers while the Al surface is micro-etched. The pretreatment is done in the first modules of the line. An alkaline zincate solution is used for activating the Al surface. For the electroless Ni plating a bath based on sodium hypophosphite is used. The rate of Ni deposition is 20µm/h. A final Au coating on the Ni is necessary to prevent oxidation and enables long-time solderability of bumps. With this Au coating a maximum Au thickness of 0.25µm can be achieved (typ. 0.05µm). The complete process flow is shown in figure 1. The quality of bumps is controlled by optical microscopy, profilometer measurements and shear tests. For detailed analysis cross-sectioning, SEM and EDX are used.

The minimal bump height is 1µm to have a closed and voidless Ni-layer. The maximal height is limited by the pad to pad spacing. The bump height must not be larger than ½ pad spacing minus 5µm to avoid short circuits between neighboring pads by over-growing Ni. A height of 5µm is recommended for FC soldering. Figure 2 shows a part of an electroless Ni/Au bumped Wafer with a pad pitch of 50µm. This meets the requirements of reliability and fast processing. The adhesion of the bumps on the Al pads depends on the pad area. For 100 x 100 µm pads the shear strength is at least 100g.

![Fig. 2: Ultra fine pitch bumping (Pitch: 50µm)](image)

The uniformity of bump height is ±2% on 4” (100 mm) wafers, ± 4 % on 8” (200 mm) wafers and ± 5 % on 12”, which is sufficient for nearly all types of applications. Detailed data on the reliability of the Al/Ni interface was
published [4]. The Ni/Au bump characteristics are summarized in table 1.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Acceptable Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer size</td>
<td>4” (100 mm) – 12” (300 mm)</td>
</tr>
<tr>
<td>Wafer backside</td>
<td>Any</td>
</tr>
<tr>
<td>Pad geometry</td>
<td>Any (square, rectangular, round)</td>
</tr>
<tr>
<td>Pad size</td>
<td>&gt; 40 µm for production (&gt;10 µm for prototyping)</td>
</tr>
<tr>
<td>Pad spacing</td>
<td>≥ 2x bump height + 10µm for production (≥5 µm for prototyping)</td>
</tr>
<tr>
<td>Metallization</td>
<td>AlSi 1%, AlSi 1% Cu 0.5% or AlCu 2%</td>
</tr>
<tr>
<td>Al thickness</td>
<td>1 µm for production (0.5 µm for prototyping)</td>
</tr>
<tr>
<td>Wafer probing</td>
<td>Before or after Ni/Au plating</td>
</tr>
<tr>
<td>Passivation</td>
<td>Defect-free nitride, oxide, polyamide, without any residues on the pads</td>
</tr>
<tr>
<td>scribeline</td>
<td>Isolated (test pads acceptable)</td>
</tr>
</tbody>
</table>

Tab. 2: Design rules for the Ni/Au bumping process

For achieving reliable and reproducible results regarding the electroless Ni/Au bumping of several types of wafers from 4” up to 12”, design rules have been defined. As pad materials AlSi 1%, AlSi 1% Cu 0.5%, AlCu 2% and other alloys of these metals were investigated. All types have been processed with good results. Nevertheless there are some restrictions on the wafers to be Ni bumped. The Al bondpad thickness should be 1µm or more in order to have sufficient Al after cleaning and activation. There are no limits to passivation thickness but the passivation must be free of defects. Cracks cause a growth of Ni which can produce short circuit. This will also occur on parts of a wafer surface which were scratched by improper handling. Ni also grows on Si which is not covered by an oxide or passivation layer. Unprotected Si in the wafer scribe line will cause plating of a Ni layer with low adhesion. Therefore the scribe line should be almost insulated, except for defined process control structures. A summary of the wafer design rules is shown in table 2 [7].

All these results and requirements can be transferred to electroless Ni/Au bumping on Cu pads. Of course the Ni/Au process has to be modified, especially the pretreatment and activation processes have to be changed for bumping on an other bond pad metallurgy.

The new electroless Ni/Au on Cu process will be qualified together with the redistribution process within the next few months by doing the necessary reliability investigations.

**Wafer Level Redistribution – “ElastoPAC”**

To start with the wafer level redistribution a redistribution design has to be made first [10, 12].

![Fig. 3: Redistribution Layout for Pac 2.1 Test Wafer](image)

As an example and a test vehicle Pac Tech’s 4 inch test wafer Pac2.1 with a peripheral layout of 200 micron pitch and a PSG passivation was used. Figure 3 shows the redistribution design for the Pac 2.1 test wafer.

<table>
<thead>
<tr>
<th>Dielectric characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material</td>
<td>Epoxy based</td>
</tr>
<tr>
<td>Thickness</td>
<td>10 µm</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>1 MHz: 4.1</td>
</tr>
<tr>
<td></td>
<td>1 GHz: 3.4</td>
</tr>
<tr>
<td>Insulating Resistance</td>
<td>10^{14} Ω</td>
</tr>
<tr>
<td>CTE</td>
<td>60 - 70 ppm°C</td>
</tr>
<tr>
<td>T_G</td>
<td>130 - 150°C</td>
</tr>
<tr>
<td>Water Absorption</td>
<td>&lt; 0,5%</td>
</tr>
</tbody>
</table>

Tab. 3: Characteristics of Photodielectric
There are two prerequisites of electroless copper metallization of a dielectric material. First, adhesion must be obtained and second, proper catalytic activation has to be achieved.

The seed layer generation takes place as a gas phase plasma process (PECVD). Therefore, a plasma reactor with a parallel plate design and a RF-powered circular substrate electrode is used. This process is developed by Atotech for direct metallization of dielectrics for future requirements in PCB industry [6] and specially adapted for wafer applications. Figure 6 shows a scheme of the PECVD chamber and gives the standard plasma parameters.

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![Fig. 5: Cross section of wafer level redistribution](image)

**Fig. 5: Cross section of wafer level redistribution**

Wafer passivation material can be SiN, SiO₂, PSG as well as PI. Additionally to our standard dielectric BSC and PI is currently under evaluation.

For full area copper deposition a seed layer formation will be followed by an electroless Cu plating batch process.

![Fig. 6: Scheme of the PECVD chamber](image)

**Fig. 6: Scheme of the PECVD chamber**

The plasma metallization consists of three different steps. In a first pretreatment step the dielectric is conditioned by plasma without roughening the surface in contrast to wet chemical processes. The second step is the deposition of a 5 - 10 nm thick transition metal layer by PECVD. In a subsequent third step, this catalytically active seed layer activates an electroless copper metallization bath.

This direct metallization by PECVD is applicable to a wide range of polymers which are used as dielectric in electronic industry like PI, epoxy resins or even fluoro polymers for high-frequency applications. It leads to very strong polymer-metal adhesion without roughening of the polymer surface. E. g. on PI adhesion of more than 20 N/cm (peel off test) is reachable.

The Cu becomes structured by an photomasking and etching process. At least the surface is covered by a solder mask and the opened Cu bond pads are NiAu bumped again.

The results of the Cu redistribution Layer for our test vehicle is shown in figure 7.
Solder bump formation can be done by solder stencil printing, where an automatic printing machine is used. Typical solder paste are Pb37Sn63 alloys with particle sizes below 20 µm. The stencil apertures are adapted to the specific application. The volume of the printed paste is determined by the aperture diameter and stencil thickness. The selection of appropriate stencil geometry is essential for printing with high yield. Special design rules have been developed for this process [7]. The subsequential solder is reflowed and flux residues are cleaned. The solder volume after reflow will be approx. 50% of the paste volume. Figure 8 shows printed solder paste after reflow in a pitch of 180 µm.

To implement the wafer level redistribution into a wafer level CSP it is necessary to increase the solder bump height. Therefore Pac Tech is using a propriety process, which cannot be shown in detail at the moment. Essentially it is necessary to use techniques like LS² and SB² for solder ball attach [8,9].

**LS² – Ball Gang Placement and Laser Reflow**

The LS² process, like it is shown in figure 9, combines 2 techniques:

1) solder ball gang placement by using a stencil
2) solder ball reflow by using a laser scanner

The advantages due to stencil printing are, the possibility to apply a higher solder volume on the redistributed pads and the much easier and more efficient flux cleaning compared to an oven reflow, because of the only locally applied laser energy, which will not effect the flux residues beneath the solder spheres. An additional advantage of a ElastoPAC as a wafer level CSP is that for encapsulation halogen-free components can be use.

The SB² is used for repair of sites with missing or bridged balls.

The whole process is comparable due to cost and process time with the stencil printing technique. The laser reflow of the solder balls has the advantage of immediately tacking the solder ball to the corresponding bond pad within the time schedule of only a few milliseconds. Due to the contactless laser scanning method the speed of the reflow of this system is optically controlled. Therefore, such a system can reflow one solder ball within only a few milliseconds. A key for the reproducible laser reflow is the control of the temperature. With the new system an accurate control of each solder ball
during reflow is possible. With the temperature control unit (TCU) via infrared feed back signal it is also possible to detect if a solder ball is existing or missing, so that an additional control of the wafer reflow and bump yield is possible.

It could be shown that with the short laser pulse self – alignment of the solder sphere will occur. Due to the short laser pulse, a reflow of the solder spheres with a thin layer of flux is possible. The control of flux thickness is not as critical compared to the oven reflow. Due to the fact that the solder sphere will immediately be tacked to the corresponding wettable bond pad and the localized temperature pulse, no shift of the solder balls is possible, even if an excessive high flux thickness is applied. This allows a highly accurate and precise placement of solder spheres on wafer level with a high yield.

**SB² – Single Ball Placement and Laser Reflow**

Preformed solder balls, which are available from several suppliers, are singulated and placed on a solderable surface (e. g. Ni/Au bumps). A short laser pulse rapidly melts the solder, leading to an excellent wetting on the substrate. No flux is required since the solder is locally protected by an inert gas (nitrogen). Figure 10 shows the principle mechanism of the placement. Solder balls can be placed on flat substrates (wafer, single dice, PCBs) as well as on complex 3D structures and Wafer Level CSP’s. The only requirements is a surface with good solder wetting properties. The main advantages of the solder ball bumping technique are:

- High flexibility
- Short set-up time
- Fluxless solder application
- Ball sizes from FC (125μm), CSP (300μm) to BGAs (760μm)
- Fine pitch ball placement (150 μm pitch)
- Several solder types possible (e. g. PbSn, AuSn)

The automatic production machine for solder ball bumping consists of a ball singulation head with z-axis control, the laser for reflow and a precise x-y-table for substrate positioning. This machine, which has a speed of 3 balls per second is applied in industry not only for flip chip applications, but also for a fluxless, low temperature stress solder ball placement in Chip Size Packages (CSP) [11].

The main cost advantage of the SB² compared to stencil printing is the low capital cost and the low set-up cost, since no additional tooling (stencil) is required. This results in a high flexibility and a fast turnover cycle, since after receipt of wafer, solder bumping can immediately start.

**Lead-free Solder and environmental Aspects**

Concentrating on the material aspects there are a lot of different opportunities due to the usage of different solder materials as well for the wafer level redistribution as for the wafer level CSP.

In the case of the LS² or SB² solder application for CSP it is easy to understand that different solder alloys, especially lead-free solder, can be implemented without any further process development or additional costs only by using the commercially available solder balls of the specific alloys.

On the other hand lead-free solders, which are currently not available for ultra-fine pitch stencil printing, can than used for solder printing of the redistributed wafers, in cause of the increased and now suitable pitch.

Preliminary results of lead-free solder printing are presented in the following.

![Fig. 11: Reflowed SnAgCu solder Bumps](image)

Figure 11 shows stencil printed SnAg4Cu0.5 solder bumps after reflow and flux cleaning on a layout with 250 μm pitch. 200μm pitch is currently under development.
Tab. 4: Results of lead-free solder stencil printing

<table>
<thead>
<tr>
<th>Lead-free bump characteristic</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shear force</td>
<td>96.75 g</td>
</tr>
<tr>
<td>Standard deviation</td>
<td>5.24 g</td>
</tr>
<tr>
<td>Shear mode</td>
<td>Bulk solder</td>
</tr>
<tr>
<td>Bump height</td>
<td>101 µm</td>
</tr>
<tr>
<td>Standard deviation</td>
<td>1.72 µm</td>
</tr>
<tr>
<td>Cleaning result</td>
<td>Excellent</td>
</tr>
<tr>
<td>Pad size</td>
<td>100 µm</td>
</tr>
</tbody>
</table>

The result is shown in figure 11 and the measured data is summarized in table 4. SnAg3.5 solder paste is also tested and for prototyping quantities available. The results are comparable with SnAgCu.

The transfer of this process on redistributed surfaces will be done and reliability results will be available soon.

Summary and Outlook

Different processes for solder ball placement and the main steps for a new low cost wafer level redistribution process were presented. Using electroless Ni as a key technology the process fulfills together with other wet chemical batch plating techniques, like electroless Cu, and the less masking steps the requirements of a low cost process.

Further advantages of electroless Ni are the selective plating on Al and Cu bond pads and the ultra fine pitch capability.

The epoxy based photodielectric makes the process capable for all wafer passivation types, which are used in industry today and offers as a plating base a reliable adhesion for the Cu redistributed bond pads and circuits. The PECVD deposition of the seed layer for electroless Cu plating opens due to the flexibility of the process beside high adhesion also perspectives for the metallization of future polymer dielectrics.

Solder application can be done by stencil printing and in the case of an wafer level CSP by LS2 method. The advantage of using LS2 due to solder alloy flexibility and reliability aspects was pointed out.

References


