A Roadmap to Low Cost Flip Chip and CSP using Electroless Ni/Au

T. Oppert, T. Teutsch, E. Zakel

Pac Tech – Packaging Technologies GmbH
Am Schlangenhorst 15 -17, Germany
Phone: +49 (0)3321/4495 -0
Fax: +49 (0)3321/ 4495 -23
e-mail: oppert@pactech.de
www.pactech.de

ABSTRACT

Flip Chip (FC) Technology is gaining an increased level of importance for a variety of applications based on Flip Chip on Board or Flip Chip in Package. The first driving force for the introduction of this Technology was the need to achieve increased speed and performance along with higher I/O count. A breakthrough, however, will be the use of flip chip due to cost reduction. For this aim it is essential to use low cost bumping techniques in combination with an assembly method compatible to existing SMT processes. The FC techniques presented in this paper are all based on an electroless Ni/Au bumping process.

This paper shows a Roadmap based on Electroless Nickel/Gold Bumping for all Flip Chip Interconnection Technologies used in industry today. Additional the Roadmap to future developments in semiconductor industry based on 300 mm wafers and the use of new pad metalisations like copper is shown. The compatibility of Electroless Nickel Bumping especially with these new technologies to be implemented in wafer manufacturing with in the next millenium shows that this key technology offers a Roadmap to Flip Chip Technology not only for the products and wafer technologies in use today but especially for the wafer technologies of the next generation.

Figure 1 shows electroless Nickel as a basis for anisotropic conductive adhesive (ACF) Flip Chip Assembly, for polymeric Flip Chip Assembly (conductive adhesive) and for soldering and direct chip attach type of applications using different solder alloys.

INTRODUCTION

For nearly all existing FC techniques a bump formation on the chip I/O is needed. Established techniques like the C4 process [1,2] do not fulfill the cost requirements for the low cost products. A selective chemical plating method can reduce bumping cost significantly since it does not require masking or metal sputtering. Additionally this technique easily allows a parallel processing of multiple wafers, leading to a high throughput.

In the FC assembly the Ni bumps fulfill the following function. They protect the Al and act as an adhesion layer and a diffusion barrier and guarantee a stable and reliable contact to the Al bondpads [5]. Besides this, which is mainly the function of an under bump metallization (UBM), the Ni can also offer a stand-off, e. g. for chip on glass (COG) using ACF [6]. The feasibility and reliability of this bumping process has been proven in a series of published technical papers.
Electroless Nickel UBM-A Roadmap to all Flip Chip Assembly Processes

Bumps become a more and more important technology for Flip Chip in Package applications like BGAs and especially Chip Size Packages. For these Flip Chip in Package applications (FCIP) low cost bumps are a key issue. Therefore the electroless Nickel bumping process is a key-technology for these applications. Figure 2 shows the relevance of bumps in Chip Size Packages. Especially the function of an additional corrosion protection by the low cost Nickel under bump metallization (UBM) is an important reliability improvement. The low cost under bump metallization offers the subcontractor packaging house the possibility to use the cost advantages of the assembly in Flip Chip Technology.

An additional important aspect of electroless Nickel bumping technology is the simplicity of the process steps which are shown in Figure 3. Therefore it can be implemented logistically in the manufacturing process as last step of the wafer semiconductor processing. In this case electroless nickel is an integral part of the frontend processing. Due to the incompatibility of the used chemicals with the semiconductor process, electroless Nickel can be implemented as a part of the probing and electrical testing respectively burn-in facility. In this case a closed fully automatic system is possible allowing the engineers in these facilities to handle the process.

A second possibility is the implementation of electroless Nickel bumping as a part of the backend engineering. Especially with the increased relevance of Flip Chip in Package (FCIP) applications, an implementation of this process as an integral part of a subcontractor assembly facility is possible. Also here the simplicity of the process, the possibility to design a fully automatic line and the high flexibility of the process allows both options.

Therefore, in the next decades we will have interesting developments and discussions between front end and back end engineering. The advantage of the implementation of Nickel bumping in front end engineering is given by the possibility of an optimal combination with electrical testing and burn-in. On the other hand the improved testing quality together with improved wafer qualities can potentially offer in the near future Solutions for known good die. An optimally tested die which does not necessary need burn-in, allows an implementation of bumping in the backend engineering. This offers a lot advantages, especially if bumping is an integral part of a packaging process.

Why use bumps in a CSP

- Protection of Al-Pad against corrosion
- Bumping increases package reliability
- Bumps provide interface for soldering or adhesive FC-joining

LOW COST BUMPS ARE KEY TECHNOLOGY FOR FLIP CHIP

Advantages of bumps for Flip Chip in Package

- Cost saving potential due to FC-Assembly
- Increased reliability
- Improved electrical performance
- Improved thermal management

Fig. 2: Relevance of Low Cost Bumps in Chip Size Packages

Following the Ni bumping a selective solder application on the wafer or the substrate is necessary for FC soldering. Concerning this, stencil printing of solder paste has highest potential for cost reduction in FC assembly.

In this paper the processes for FC assembly using electroless Ni and eutectic solder are described. The electroless Ni and the Ni-Solder FC interconnection system is investigated with regard to solderability, mechanical properties (adhesion) and
resistivity. All investigations in this paper are related to eutectic (Pb 37% Sn 63%) or near eutectic solder (2% Ag).

ELECTROLESS Ni/Au BUMPING

The chemical bumping process is wet-chemical and maskless [3]. With the developed manufacturing process all types of wafers can be bumped with a standard process in good quality. In a bumping line wafers from 4” (100 mm) to 12” (300 mm) diameter can be plated.

The key for a successful and reproducible manufacturing process is in the used chemicals and equipment. The electroless Nickel bumping process can be performed with standard chemicals available on the market for simple test structures and test dies without electrical inner circuitry. However, when applied to functional wafers with complex inner electrical structures, different metallization and different passivations, the process requires specific proprietary chemical compositions for a reproducible and reliable result. Here lays the key to electroless Nickel implementation in production. This is an explanation for the multitude of investigations and research projects in industry and in institutes which did not lead to a direct manufacturing process in the past.

In Berlin a concentrated team of two to three engineers has been constantly working on the process since 1989 and permanently performing further development of this process, leading finally to an industrial manufacturing process. An other key to a reliable subcontractor bumping is in the capability to handle wafers from different sources with different qualities of metallization and passivation. Here an experience based of four years in bumping of about 100 wafer types coming from different sources is a key to a manufacturing process. Beside the specific chemistry and the control of the used chemistry it is necessary to have appropriate bumping equipment.

Electroless Nickel is used in industry for a series of applications in which Al work pieces are plated with Ni. The equipment available for these standard processes based on large work pieces or printed circuit boards is not suitable for wafer bumping. In order to fulfill the specific requirements for wafer bumping a new modular electroless Ni wafer bumping line has been developed. Figure 4 shows the modular concept of the electroless Ni bumping line which can handle wafers in semi-automatic or in fully automatic modus. Each module can take batches of 25 wafers 8” or 10 wafers 12”.

Such processing is a key to the extremely high throughput of this bumping line which again determines the overall cost of the bumping process.
Ni bumping process steps

First, in order to prevent Ni plating, the wafer backside has to be covered by a stable resist prior to the chemical bumping process. The next step is a treatment in an Al cleaner which removes oxide layers while the Al surface is micro-etched. An alkaline zincate solution is used for activating the Al surface. For the electroless Ni plating a bath based on sodium hypophosphite is used. The rate of Ni deposition is 20µm/h. A final Au coating on the Ni is necessary to prevent oxidation and enables long-time solderability of bumps. A maximum Au thickness of 0.25 µm can be achieved. The complete process flow is shown in figure 5. The quality of bumps is controlled by optical microscopy, profilometer measurements and shear tests. For detailed analysis cross-sectioning, SEM and EDX are used.

Bump Characteristics

The minimal bump height is 1µm to have a closed and voidless Ni-Layer. The maximal height is limited by the pad to pad spacing. The bump height must not be larger than ½ pad spacing (plus 10µm for security) to avoid short circuits between neighboring pads by overgrowing Ni. A height of 5µm is recommended for FC soldering. This meets the requirements of reliability and fast processing. The adhesion of the bumps on the Al pads depends on the pad area. For 100 x 100 µm pads the shear strength is at least 100g. A thin Au cover layer protects the Ni from oxidizing and keeps it solderable. It can be adjusted to up to 0.25 µm (typ. 0.05µm).

The uniformity of bump height is ± 2% on 4” (100 mm) wafers and ± 4% on 8” (200 mm) wafers, which is sufficient for nearly all types of applications. Detailed data on the reliability of the Al/Ni interface was published [5]. The Ni/Au bump characteristics are summarized in table 1.

<table>
<thead>
<tr>
<th>Bump characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Recommended height</td>
<td>5 µm</td>
</tr>
<tr>
<td>Maximum height</td>
<td>&lt;½ pad spacing</td>
</tr>
<tr>
<td>Material</td>
<td>NiP 10%</td>
</tr>
<tr>
<td>Resistivity</td>
<td>70 µΩcm</td>
</tr>
<tr>
<td>Hardness</td>
<td>550 mHV</td>
</tr>
<tr>
<td>Adhesion to Al at 100 x 100 µm² pad</td>
<td>&gt;100g (typ.150g)</td>
</tr>
<tr>
<td>Au coating thickness</td>
<td>0.05 – 0.25 µm</td>
</tr>
</tbody>
</table>

Tab.1: Electroless Nickel Bump characteristics

Wafer Design Rules

Based on the experience, gained by the processing of several types of wafers, design rules have been defined. As pad materials AlSi 1%, AlSi 1% Cu 0.5%, AlCu 2% and other alloys of these metals were investigated. All types have been processed with good results. Nevertheless there are some restrictions on the wafers to be Ni bumped. The Al bondpad thickness should be 1µm or more in order to have sufficient Al after cleaning and activation. There are no limits to passivation thickness but
the passivation must be free of defects. Cracks cause a growth of Ni which can produce short circuit. This will also occur on parts of a wafer surface which were scratched by improper handling. Ni also grows on Si which is not covered by an oxide or passivation. Unprotected Si in the wafer scribe line will cause plating of a Ni layer with low adhesion. Therefore the scribe line should be almost insulation (thin thermal oxide is sufficient), except for defined process control structures. Furthermore the pad spacing has to be at least 20µm to prevent shorts by overgrowing Ni. A summary of the wafer design rules is shown in table 2.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Acceptable Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer size</td>
<td>4” (100 mm) – 8” (200 mm)</td>
</tr>
<tr>
<td>Wafer backside</td>
<td>Any</td>
</tr>
<tr>
<td>Pad geometry</td>
<td>Any (square, rectangular, round)</td>
</tr>
<tr>
<td>Pad size</td>
<td>&gt; 40 µm for production (&gt;10 µm for prototyping)</td>
</tr>
<tr>
<td>Pad spacing</td>
<td>&gt; 20 µm for production (&gt;5 µm for prototyping)</td>
</tr>
<tr>
<td>Metallization</td>
<td>AlSi 1%, AlSi 1% Cu 0.5% or AlCu 2%</td>
</tr>
<tr>
<td>Al thickness</td>
<td>1 µm for production (0.5 µm for prototyping)</td>
</tr>
<tr>
<td>Wafer probing</td>
<td>Before of after Ni/Au plating</td>
</tr>
<tr>
<td>Passivation</td>
<td>Defect-free nitride, oxide, polyamide</td>
</tr>
<tr>
<td>scribe line</td>
<td>Insulating (test pads acceptable)</td>
</tr>
</tbody>
</table>

Table 2: Summary of design rules for Ni/Au bumping manufacturing process.

**SOLDER APPLICATION**

For solder application two methods are used: solder paste printing and placement of preformed solder balls (solder ball bumping SB²).

**Solder Printing**

For solder paste application an automatic printing machine is used. For a manufacturing process of wafer level stencil printing a special workholder and wafer handling system was developed. Typical solder pastes are PbSn63 or PbSn61Ag2 alloys with particle sizes below 20 µm. The stencil apertures are adapted to the specific application. The volume of the printed paste is determined by the aperture diameter and stencil thickness. The selection of appropriate stencil geometry is essential for printing with high yield. Special design rules have been developed for this process. The subsequent solder is reflowed under nitrogen and flux residues are cleaned (figure 6). The solder volume after reflow will be approx. 50% of the paste volume.

**Laser Solder Ball Bumping (SB²)**

For rapid prototyping, fine pitch applications and solder deposition on 3D structures a novel solder application technique has been developed and implemented in a production tool. Preformed solder balls, which are available from several suppliers, are singulated and placed on a solderable surface (e.g. Ni/Au bumps). A short laser pulse rapidly melts the solder, leading to an excellent wetting on the substrate. No flux is required since the solder is locally protected by an inert gas (nitrogen). Figure 7 shows the principle mechanism of the placement. Solder balls can be placed on flat substrates (wafers, single dice, PCBs) as well as on complex 3D structures. The only requirements is a surface with good solder wetting properties. The main advantages of the solder ball bumping technique are:

- High flexibility
- Short set-up time
- Fluxless solder application
- Ball sizes from FC (125µm), CSP (300µm) to BGAs (760µm)
- Fine pitch ball placement (150 µm pitch)
Several solder types possible (e.g. PbSn, AuSn)
• For 3D structures (3D Memory Modules, 3D sensors suitable)

Cost calculation show, that solder ball bumping is a competitive method in a production environment, especially if a high flexibility and a fast turnover cycle is required.

Due to its high flexibility, the solder ball bumper is also used in our process for repair of defective solder bumps and solder bridges resulting from stencil printing.

Metallurgical considerations of electroless Nickel UBM

Compared to copper, nickel has a significantly lower dissolution rate in molten solder (Ni dissolves by a factor of 30 slower than Cu). Also the growth rate for the formation of Ni-Sn intermetallics is significantly lower compared to Cu-Sn intermetallics. This shows, that Ni has a higher potential for a further reliability improvement- especially for automotive and harsh environment applications than Cu. The use of electroless Ni-bumps in automotive engine control unit has been successfully demonstrated /8/.

Multiple reflows using electoless Ni UBM

In a production environment the Ni/solder interface has to withstand several reflows, e.g. further SMT reflows, assembly of BGA, rework. Test dice (2.4 x 2.4 mm²) with 64 I/Os in area configuration and 300µm pitch (pad size 100 x 100 µm) were used in order to investigate the reliability of soldered FC joints on electroless Ni. By the symmetrical pad design a simple die-to-die assembly was possible. All dice were plated with 5 µm Ni/Au. PbSn61Ag2 solder was applied to some dice by stencil printing. They were placed on the other dice (only with Ni/Au) and reflowed using flux. Each reflow was performed under nitrogen with a peak temperature of 230°C for a period of 40s. the strength of solder joints was tested after 1,2,4,6,8 and 10 reflows by pulling the dice apart in an Instron tester. For each number of reflows 4 die-to-die assemblies were tested.

The pull forces per FC bump, calculated by dividing the pull force per die by the number of bumps (64 I/O), are presented in figure 12. Pull force/bump was always higher than 70g for the 100 x 100 µm bumps. The vertical bars

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**Fig. 7: Principle of solder ball bumping production tool using laser (SB²)**

The high speed production machine for solder ball bumping consists of a ball singulation head with z-axis control, the laser for reflow and a precise x-y-table for substrate positioning. This machine, which has a speed of 3 balls per second is applied in industry not only for flip chip applications, but also for a fluxless, low temperature stress solder ball placement in Chip Size Packages (CSP) /8/, /9/ and for special sensor packages.

The main cost advantage of the SB² compared to stencil printing is the low capital cost and the low set-up cost, since no additional tooling (stencil) is required. This results in a high flexibility and a fast turnover cycle, since after receipt of wafer, solder bumping can immediately start.

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**Capital cost for Solder Ball Bumping requires:**

1. Solder Ball Bumping machine

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**Capital cost for stencil printing requires:**

1. Automatic high precision stencil printer
2. Stencil cleaning unit
3. Analytical equipment for solder paste rheology
4. Nitrogen reflow oven
5. Flux cleaning station
6. Wafer optical inspection equipment
indicate lowest and highest force. Since this test is very sensitive to non-perpendicular pull, the scatter of forces is large. However the results show that even 10 reflows do not influence significantly the mechanical stability of solder joints on electroless Ni bumps. Additional a new testing method for Flip chips using a torsion tester was applied. The developed equipment results in a better accuracy of the mechanical properties of FC-interconnections. A more detailed description of the measurement principle is given in /11/.

Fig.8: Stability of FC joints vs. number of reflows

Reliability of FC-Assemblies using electroless Nickel UBM

The reliability of Flip Chip assemblies using electroless Ni/Au under bump metallization has been previously shown in a series of publications made by different institutes and companies. The basic reliability of the interface between Al and Ni respectively Ni and solder respectively Ni/Au and polymeric interfaces has been proven. A Flip Chip assembly using a electroless Ni/Au under bump metallization and a solder bump applied by stencil printing or SB² will show comparable basic reliability data as a geometrically equivalent electroplated solder bump.

The reliability of Flip Chip assemblies today is more and more determined by the assembly parameters, assembly yield, quality of the used substrate materials, design rules of pad opening versus bump size and the properties of the used underfill process. A key to the reliability of a Flip Chip on an organic printed circuit board is the underfill process, the mechanical properties of the used underfill material and the flow characteristic, voids etc. As parameters of the Flip Chip assembly process the used fluxes and especially flux residues around the bumps reduce reliability in thermal cycling tests. These reliability parameters are common to all Flip Chip assembly processes independent of the applied bumping technology.

As a summary of investigations using electroless Ni/Au bumps known so far, it was proven that they result in a extremely reliable interconnection. If the assembly process and the underfill process is performed according to the state of the art in industry today (Figure 9), the FC interconnect will withstand 2000 and more thermal cycles.

Fig.9: Reliability of FC-Assembly using electroless solder bumps

Comparable results are obtained with electroless Ni in combination with isotropic conductive adhesives. These materials are of interest in Smart Card applications. The mechanical stability of the Flip Chip Interconnections during mechanical bowing and torque of the Smart Card body is of essential importance. The reliability of electroless Ni bumps in Smart Card applications have also been demonstrated. The interconnection will pass the standard reliability tests of Smart Card industry.

Finally electroless Ni/Au has an extremely high potential to replace the cost intensive electroplated Au bumps used in LCD Chip on glass applications today. This is an application in combination with anisotropic conductive adhesives and fine pitch bumps in a pitch of 50-70 µm. The basic aspects of the reliability of electroless Ni/Au bumps in combination with anisotropic conductive adhesives has been demonstrated.

The reliability of these interconnects is mainly determined by the quality of the used anisotropic conductive materials and the quality of the assembly process and substrate.
Figure 10 shows the reliability performance of a Flip Chip assembly using electroless Ni and anisotropic conductive film. The degradation of the contact resistance is due to the properties of the polymeric matrices in the ACF and not determined by the bump material. In these interconnects thermal cycling turns out to be not as critical as high temperature humidity testing. In these tests the water absorption of the ACF polymeric matrix determines the reliability. These results show that electroless Ni is a reliable interconnection for a high quality Flip Chip using ACF.

SUMMARY

In summary this paper shows that electroless Ni/Au bumps offer a powerful Roadmap for Flip Chip interconnections on board (FCOB) and in package (FCIP) in the next millennium. The Roadmap of Flip Chip assembly using soldering techniques, conductive adhesives and anisotropic conductive adhesives could be shown. Aspects regarding the of implementation of electroless Ni/Au in backend and frontend engineering have been discussed. The process data available so far, have been presented together with some selected reliability data on different assembly techniques. The main challenges of electroless Ni/Au as an under bump metallization in a near future is reduction of pitch to 50 µm and the development of solder application techniques in this fine pitch area. An additional challenge will be a strategy of implementation of test and known good die in a process flow for electroless Ni/Au bumping.

References


