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The Flip Chip Technology has an increasing market for Flip-Chip-In-Package and Flip-Chip-On-Board applications. European requirements are basically focusing on smart cards, smart labels and automotive microelectronic products. The availability of bumped dies at reasonable cost is essential for all Flip Chip applications.
Pac Tech has recently opened a new Subcontractor Bumping Facility with a bumping-capacity of 100.000 wafers, up to 8”, per year.
The bumping process, which is based on an electroless Ni/Au Under Bump Metallization (UBM) and solder application by stencil printing on wafer level allows a significant cost reduction in comparison to electroplating. The Ni/Au-bumps are applied for both – soldering and adhesive joining flip chip interconnections.

Ni/Au-Bumping-Line in cleanroom class 10.000
The process meets the aggressive cost targets in smart card and smart label applications. On the other hand this bumping process meets the high reliability requirements for automotive microelectronic products and Flip Chip in Package (e.g. CSP).

Additional to Subcontractor Wafer Bumping, Pac Tech offers support in Flip Chip assembly, prototyping design of substrates and first products. For this, a Flip Chip User Group has been formed.
Presentations on Pac Tech’s Flip Chip Technology will be given in 1999 during Semicon Europe, Semicon Singapore and Semicon West.
For more detailed information regarding Wafer Bumping and Flip Chip please contact: