INTRODUCTION

Modern microelectronic products require packages that address the driving forces of reduced size and weight, as well as increased performance at high frequencies. Flip-chip and direct chip attach on the board offer straightforward solutions to these growing demands. This paper describes a low-cost electroless nickel/gold (Ni/Au) under-bump metallization (UBM) and a wafer-level redistribution (RDL) process based on electroless copper circuitization.

By Ron Blankenhorn, Pac Tech USA, Santa Clara, Calif., and Thomas Oppert, Pac Tech GmbH, Nauen, Germany

A key requirement for flip-chip is a bumped wafer, which may be produced by any of several technical methods, including electroplating, electro-less bumping and evaporation.

Electroless bumping offers, we believe, the most elegant and least expensive solution of the bumping methods currently available.

The key to flip-chip success is based on several factors, including ultrafine-pitch bumping at a pitch less than 200 µm, which is shrinking to 100 µm and smaller. Perhaps the true key to flip-chip success in ultrafine applications is the availability of PWBs with a pitch under 200 µm.

Wafer-Level Redistribution

Most wafers are designed for wirebonding with peripheral pad configurations in ultrafine pitch. These, however, are not ideal solutions for flip-chip. To prepare wafers for flip-chip packaging, one interim solution consists of the wafer-level redistribution of the bond pads, from peripheral to area-array pads with larger sizes and a relaxed pitch.

Low-cost electroless nickel/gold (Ni/Au) UBM and a wafer-level RDL process based on electroless copper circuitization is described in this article.

The process includes the use of a novel, plasma-enhanced chemical vapor deposition (PECVD) process. This process deposits a bifunctional nanolayer acting as an adhesion promoter and as a catalyst for electroless copper deposition.

The techniques described are suitable for all wafer passivation types used in the semiconductor industry today. The complete RDL process is based on batch processing and fewer masking and photo-imaging steps. Using the electroless nickel process and wafer-level stencil-solder printing makes the process highly cost-efficient, with a large-volume manufacturing capability.

A standard technology for a wafer RDL process is based on sputtering and the use of high-end dielectrics, such as benzo-cyclo buthen (BCB) or polyimide. These dielectrics are associated with high cost. On the other hand, a process that avoids sputtering technology can produce major cost savings for wafer-level RDL.
Semi-Additive Approach

In the first step of our proprietary, semi-additive approach to wafer-level RDL, the bond pads on the wafer are passivated with electroless Ni/Au. (The process steps for electroless Ni/Au are well known in the industry.) After development, the process was implemented in a high-volume production line1 (Figure 1).

The process employs wet-chemical dipping procedures in well-controlled chemicals and environments, avoiding sputtering and photo-imaging steps. In step two, a 5-10 µm-thick dielectric (optionally 15 µm), is applied at the wafer level.

Ideally, this dielectric is a photo-imageable material. After photo-imaging, the diameter is opened in the area above the bond pads, which were previously protected with electroless Ni/Au bumps.

In the next steps, the dielectric is prepared with a special catalytic material that provides, in addition to its catalytic properties, optimum adhesion to the subsequent electroless copper plating. Electroless copper plating is done in batch processing of 25-50 wafers.

Batch Processing

The main advantage of using electroless copper plating over electroplating is the ability to batch process, which enables extremely high throughput and reduces process costs.

The electroless copper can be deposited in its full thickness (up to 5 microns) with a special, high-speed copper base.

After plating to the desired and required thickness, which is 5 µm on the full-wafer scale, the electroless copper film is etched after a second photo-imaging step is applied.

For a wafer-level redistribution on a wafer-level CSP, an additional solder mask is applied with a second dielectric layer. The dielectric is photo-imaged in a third process step and opened in the area above the solder bumps that will be attached to the PWB.

A final step for wafer-level RDL is the application of an additional solid-state bump. This bump may be electroless Ni/Au. The electroless Ni/Au bump on the redistribution wafer is ideally suited for ACF or conductive adhesive joining.

Solder Spheres

Alternatively, for soldering processes, solder spheres are required. To improve the reliability and thermal fatigue resistance of the redistributed flip-chip layout, solder spheres with a large diameter are preferred.

Spheres of 300 µm diameter in a 500 µm pitch cannot be applied with wafer-level stencil printing. This printing is limited to larger pitches of 300 µm-diameter solder spheres.

However, for 500 µm pitch, wafer-level ball placement and reflow is the preferred process.
Electroless Ni/Au Bumping

Electroless Ni/Au bumping is a wet-chemical, maskless process. With the developed manufacturing process, all types of wafers can be bumped with a standard process, yielding excellent quality. In a specially designed bumping line, wafers from 100 mm to 300 mm diameter can be plated(1,4).

The key to a successful, reproducible and reliable manufacturing process lies in the chemicals and equipment used. For functional wafers with complex inner electrical structures, different metallization and different passivations, the process requires specific proprietary chemical compositions and know-how.

Before the wafers can be metallized in the line, the back-side of the wafer must be covered by a stable resist preceding the chemical bumping process. This is the key to electroless nickel implementation in production.

The next step is treatment of the pads in an aluminum cleaner that removes oxide layers while the Al surface is microetched. Pretreatment is done in the first modules of the line. An alkaline zincate solution activates the Al surface. For the electroless Ni plating, a proprietary chemical solution is employed.

A final Au coating on the Ni is necessary to prevent oxidation and to enable the long-time solderability of bumps. The quality of bumps is controlled by optical microscopy, profilometry and shear tests. For detailed analyses, cross-sectioning, SEM and EDX are used.

The minimum bump height is 1 µm for a closed and voidless Ni layer. The maximum height is limited by the pad-to-pad spacing. A 5-micron height is recommended for flip-chip soldering.

Figure 2 shows part of an electroless Ni/Au bumped wafer with a pad pitch of 50 µm, which meets the requirements for reliability and fast processing. The adhesion of bumps to the Al pads depends on the pad area. (Detailed data on the reliability of the Al/Ni interface have been published(2).)

Design rules have been defined for achieving reliable and reproducible results in the electroless Ni/Au bumping of several types of wafers from 100-300 mm.
Pad Materials

Al, AlSi, AlSi Cu or AlCu can all be used as the pad material. Nevertheless, some restrictions exist on the wafers to be Ni bumped. The Al bond pad thickness should be 1 µm or more to leave sufficient Al after cleaning and activation.

No limits to passivation thickness exist, but the passivation must be free of defects. Cracks cause a growth of Ni, which can produce a short circuit. This will also occur on parts of a wafer surface that have been scratched by improper handling. Ni also grows on Si not covered by an oxide or passivation layer. Moreover, unprotected Si in the wafer-scribe line will cause plating of a Ni layer with low adhesion. The scribe line should therefore be almost insulated, except for defined process-control structures.

These results and requirements can be transferred to electroless Ni/Au bumping on Cu pads. Of course the Ni/Au process must be modified, especially the pretreatment and activation processes, which must be changed for bumping on another bond-pad metallurgy.
Test Wafer

We developed a test vehicle with a peripheral layout of 200 microns pitch and PSG passivation. Figure 3 shows the redistribution design for the test wafer.

Initially the redistribution starts with Ni/Au bumping of the Al bond pads up to a Ni height of 5 µm (Figures 4, 5). An epoxy-based dielectric is then spun on the existing wafer passivation.

Wafer passivation material can be SiN, SiO2 or PSG, as well as polyimide. In addition to our standard dielectric, BSC and polyimide are under evaluation. For full-area copper deposition, a seed-layer formation will be followed by an electroless Cu plating batch process.

Prerequisites

There are two prerequisites for electroless copper metallization of a dielectric material: First, adhesion must be obtained; second, proper catalytic activation must be achieved.

The seed-layer generation takes place as a gas-phase plasma process (PECVD).
Therefore, a plasma reactor with a parallel plate design and an RF-powered circular substrate electrode are used. This process has been developed for direct metallization of dielectrics for future requirements in the PWB industry(3) and specially adapted for wafer applications. Figure 6 shows a schematic of the PECVD chamber and gives standard plasma parameters.

The plasma metallization consists of three different steps. In a first pretreatment step, the dielectric is conditioned by plasma without roughening the surface, in contrast to wet-chemical processes. The second step is the deposition of a 5-10 nm thick transition metal layer by PECVD. In a subsequent third step, this catalytically active seed layer activates an electroless copper metallization bath.

This direct metallization by PECVD is applicable to a wide range of polymers that are used as dielectrics in the electronics industry, such as polyimides, epoxy resins or even fluoropolymers for high-frequency applications.

![Figure 7. Cu redistribution layer.](image1)

![Figure 8. Stencil printed solder bumps.](image2)

**Strong Polymer-Metal Adhesion**

Direct metallization leads to very strong polymer-metal adhesion without roughening of the polymer surface. For example, a polyimide adhesion of more than 20 N/cm (peel-off test) is reachable.

The Cu becomes structured by a photomasking and etching process. The surface, at a minimum, is covered by a solder mask, and the opened Cu bond pads are Ni/Au bumped again. Results of the Cu redistribution layer for our test vehicle are shown in Figure 7.

Where an automatic printing machine is selected, solder-bump formation can be achieved by solder stencil printing.

Typical solder pastes for this application are eutectic PbSn and SnAgCu alloys with particle sizes below 20 µm.

Stencil apertures are adapted to the specific application, while the volume of the printed paste is determined by the aperture diameter and stencil thickness.

The selection of appropriate stencil geometry is essential for printing with high yields, and special design rules have been developed for this process(4).

**Solder Reflow**

The subsequent solder is reflowed and flux residues are cleaned. Solder volume after reflow will be approximately 50% of the paste volume. Figure 8 shows printed solder
Summary

This new, low-cost wafer-level redistribution process employs electroless Ni as a key technology. This process fulfills the requirements for low cost, as do other wet-chemical batch-plating techniques like electroless Cu, and also features fewer masking steps than other RDL.

Further advantages of electroless Ni are selective plating on Al and Cu bond pads and ultrafine-pitch capability. The epoxy-based photodielectric makes the process suitable for all wafer-passivation types used in industry today. Owing to the flexibility of the process, the PECVD deposition of the seed layer for electroless Cu plating opens, in addition to high adhesion, the potential for metallization of future polymer dielectrics.

References


4. Pac Tech web page: pactech.de