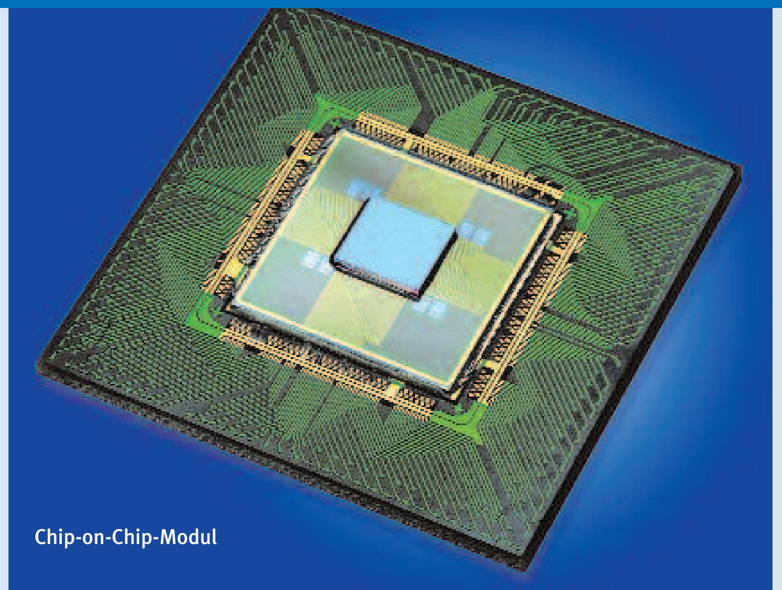


Chip-on-Chip-Modul

New packaging technologies – taking their time, but now things are moving

From package to system

The old familiar technologies, especially wire bonding, may still dominate the world of packaging, but there are signs of change. Only area packages are showing growth figures. Apart from that the system idea is in the air. ICs, packages and systems may no longer be considered separately from one another.

»Packaging and system integration is becoming increasingly significant«, says Harald Pötter, head of the smart system integration applications center at the Fraunhofer IZM. Heterogeneous integration in particular will in future develop the link between electronics and the particular applications. Package costs will account for a bigger share of overall costs. Pötter reckons they will remain constant per pin, i.e. not drop as fast as the number of pins increases.

Packaging is by no means still just a matter of applying molding compound to a chip and housing it. Heterogeneous integration is the watchword, by means of which the nanoworld of ICs is to be joined to the systems with which we ultimately communicate. System in package (SiP) is another expression for it.

Actually a rapid redirection was already forecast for packaging at the end of the last decade, in Europe too. At that time experts were convinced that socalled advanced packaging would commence its triumphal march. This includes the flip-chip and chip scale packaging (CSP) technologies that would supposedly make wire bonding superfluous. In CSP additional wiring layers (redistribution layers) are deployed on the surface of the chip so that the bonds can be distributed as bumps over the entire top of the chip. That puts CSPs among the area packages, which also include BGAs, although these are attached on the rear to a substrate under which in turn the balls are arrayed.

CSP technology was meant to take care of a number of problems: propagation delay through the bond wires, and problems from electromagnetic radiation, because at high frequencies the bond wires act like tiny antennas. Fabricating redistribution layers calls for processes that are much more like fabricating the ICs themselves (frontend) than traditional chip assembly (backend). For which reason numerous experts reckoned that the backend would come closer to the wafer fab, and at least part of the packaging, the majority of which is now carried out in Asian countries, would come back to the fabs, to Europe too.

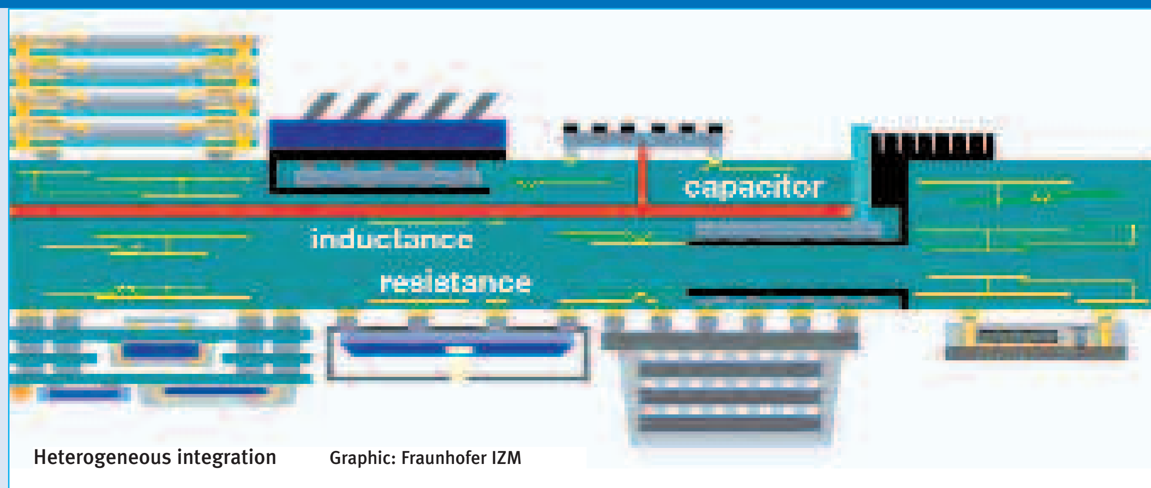
And what has become of all the predictions? 3D integration is taking place. In cellphones for instance you find chips in which several dies, like different kinds of memory, are stacked on top of one another. There are numerous other examples, like in smart power where different dies are set on a substrate next to one another or stacked one on the other. Nevertheless, interconnection — quite differently to what might be expected — is still for the most part by the good old bond wires. The reason is that wire bonding is a technology in which the manufacturers have accumulated in-depth knowledge and experience. They have full command of it, and it is considered simple, even if a number of stacked dies with hundreds of bond wire connects do not exactly look so simple. And if a technology is good and reliable, manufacturers will naturally stick to it for as long as possible.

But still the tide seems to be turning. »Although wire bonded systems today easily account for the biggest share, it's only area packages that are registering growth. So it's only a matter of time before they take the place of wire bonded types«, forecasts Rolf Aschenbrenner, head of chip interconnection technologies at the Fraunhofer IZM. In the long run the optimists would thus be proven right, even if they had had to wait ten years for the evidence. In any case, major semiconductor manufacturers were now working on it. And he is convinced that advanced packaging will not migrate from Europe.

There are several reasons for this, the way he sees it. Investment in chips fabricated with 65 nm structures and smaller was so high that only enormous quantities would justify it. »For less volume there's no way out except clever partitioning«, concludes Aschenbrenner. And that meant stacking a number of chips with relatively large-sized structures on top of one another – but using the very latest methods like through-vias. The keyword here was »More than Moore« instead of »More Moore«.

SiPs are custom

Compared to systems on chip (SoCs), systems in package (SiPs) exhibit a number of advantages in medium and smallish quantities. They too are very small, but the functional parts can be fabricated in the technology that is optimal for them. At the same time this means that the packaging technology must close up to the customer, because systems of this kind are custom. »The result of system integration is



Heterogeneous integration Graphic: Fraunhofer IZM

Thomas Oppert, PacTech

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Oswin Ehrmann, IZM

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"System integration will lead to both design and increasingly also manufacturing of systems on the basis of advanced packaging technology taking place in Europe."

that you see both development and, increasingly, fabrication in Europe«, reckons Aschenbrenner. And because packaging is heading in the direction of application-specific solutions, opportunities are opening up for smaller enterprises like PacTech in Nauen and MPD in Dresden. While PacTech offers bumping services for wafers, besides developing and building machines for packaging, MPD concentrates on single- and multichip packages.

As Thomas Oppert, vice president marketing & sales at PacTech, explains, the demand for wafer bumping services has risen very significantly in the last three years. As a result the company doubled its workforce between 2003 and 2004 and again from 2004 into 2005. PacTech currently employs 150 persons, has operated a plant in Silicon Valley since 2001, and a facility in Malaysia is now commencing production. In Nauen the company is setting up a second line to process 12 inch wafers, which are already being handled by the operations in the USA and Malaysia. Each site has capacity of 600,000 8 inch wafer equivalents.

PacTech notices the increased demand for wafer bumping both in services, which contributed some 25% to turnover of 15 million euros in the last fiscal, and in machines, which accounted for the remaining 75%. The company's customers include nearly all big semiconductor manufacturers and suppliers, to the telecommunications industry for example, who either require bumping services or purchase machines and license the PacTech process.

Here PacTech has specialized in wet chemical systems for nickel-gold underbump metalization and associated machinery for spin coating, plasma and flux cleaning.

PacTech is highly successful in serial solder ball placement. Balls down to a diameter of 60 µm can be melted on by laser with a pitch of 100 µm. »3D contacting for read/write heads of harddisk drives wouldn't be possible in any other way, so all big harddisk manufacturers are customers of ours«, enthuses Oppert. Other applications include camera modules and cardiac pacemakers.

PacTech has also developed a machine that does not perform solder ball placement by stainless steel masks (gang ball placement) but instead uses a new technique to place balls down to 80 µm in diameter. Common techniques only go down as far as 250 µm. Overall he is very optimistic, not only where advanced packaging itself is concerned, but also regarding the site: »There are companies that have already returned to Europe to carry out their packaging processes.«

MPD in Dresden is part of Silicon Sensor International AG, which has an 85% holding in Micro Sensors GmbH. Since the outset of the year Micro Sensors has been developing and marketing products like pressure sensors for the automobile industry and camera systems for security applications and automobiles. The sensors for the systems are primarily manufactured by MPD.

Likewise located in Dresden is KSW Microtec, whose services include wafer bumping and packaging. Established in 1994 to commercialize and further develop polymer flip-chip technology, the company now rates as a leading world supplier of RFID components for standard and special applications such as logistics and local public transportation, and for security requirements like contactless credit cards and access systems. In VarioSens, an RFID temperature data logger, KSW has become a forerunner in active label technology. Adding an eco-friendly battery and a sensor controlled chip turns the passive label into a semi-active one that can be found in use in very many segments to monitor products sensitive to temperature. In 2004 the company started volume production of UHF bag tag inlays, which are used at Las Vegas and Hong Kong airports. KSW also delivered the entire inlays for tickets to the 2006 Soccer World Cup.

Interesting too is a development from the Binder company: a wireless RF module measuring 20 x 20 x 10 mm powered by a replaceable 3 V lithium battery. This module detects temperature and humidity, transmitting the data in the license-free 2.4 GHz band. Its transmission protocol is ZigBee (802.15.4). The SiP consists of an electronics layer with the wireless part, sensors and actuators (LEDs and wireless antenna) on top. Inside is a RISC controller with peripheral circuitry. Programs can be saved in a 128 kbyte flash memory and 4 kbyte RAM, data in an EEPROM. The underside of the module forms the battery layer, with the battery holder and pads for contacting 16 digital I/Os, four open-collector outputs and four analog inputs.

On the way to becoming an ODM is Berlin-based AEMtec, which spun off from Infineon in 2000 and now employs 120 persons. As a provider of optical, mechatronic and electronic multichip modules in mixed technologies, AEMtec combines SMT, BGA/CSP-COB and flip-chip on all common substrates, from PCBs through film, glass and ceramic to wafers. All products are custom, and AEMtec offers the entire value-added chain from consulting through to shipment of fully tested modules. Annual quantities range between 1000 and way over 500,000 pieces. Although AEMtec cooperates with Fabrinet in Bangkok, the company considers it extremely important to show local presence. »This is where the developments happen.

With complex products like SiPs and advanced packages it's essential to be where the customer is, right through to preseries and volume manufacture«, says Matthias Lorenz, customer application support manager of AEMtec. He admits that advanced packages are only just beginning to penetrate the market, but »things are finally starting to pick up — for a year now there's been increased demand after a long period of stagnation.«

To simplify things for customers finding their way into advanced packaging, AEMtec has devised a cost model, based on quantity and batch size, for the first development phase of new modules and packages that compares Al and Au wire bond technologies besides comparing cost with flip-chip assembly.

For given boundary conditions different technology variants can thus be presented to the customer in this leadup phase. And they can be compared and discussed in terms of rationalization and technology potential for the next product generation. Through its competent network partners AEMtec also has access to diverse specialized and future-going technologies, and can conduct thermal and electric simulation of complex modules early on in their development for example.

The persuasion effort

So there definitely are areas where interesting things are going on in the way of packaging. But what is still needed is a persuasion effort. Because when users like automakers call for reliability of less than 1 ppm, they are reluctant to indulge in technologies they know so little about. And Oswin Ehrmann, head of wafer level packaging at the Fraunhofer IZM, confesses that a development effort is also necessary, especially at the polymer/metal interface. How do damp and vibration affect the boundary between metal and plastic for example? (See box)

The Fraunhofer IZM has already shown what advanced packaging is capable of. For the Atlas project of CERN the institute built pixel detectors: ICs with a pitch of 50 x 120 µm with 2800 bumps, and 16 such ICs on one detector element. So each element totals 46,000 bumps on an area of 7.5 x 2 cm. For this effort CERN even awarded the Fraunhofer Society the supplier's prize. »Advanced packaging is reliable in large quantities, we've certainly demonstrated that to industry«, says Ehrmann.

Another example is cooperation of the Fraunhofer IZM with the Bundesdruckerei in the security lab on security documents in which a chip is deposited in one of ten films. For this the chips have to be slimmed down to just 10 µm. That is in fact not the biggest problem. What is much more difficult is actually processing such thin chips and providing them with bumps. This is being conducted on a laboratory scale at the moment, but the IZM's Aschenbrenner says the project is already very close to application.

At any rate, Harald Pötter of the smart system integration applications center at the Fraunhofer IZM is sure that there is now going to be stronger demand for advanced packaging from the likes of automotive and medical engineering, and that European and especially German industry is well prepared for it. (ha) ❐