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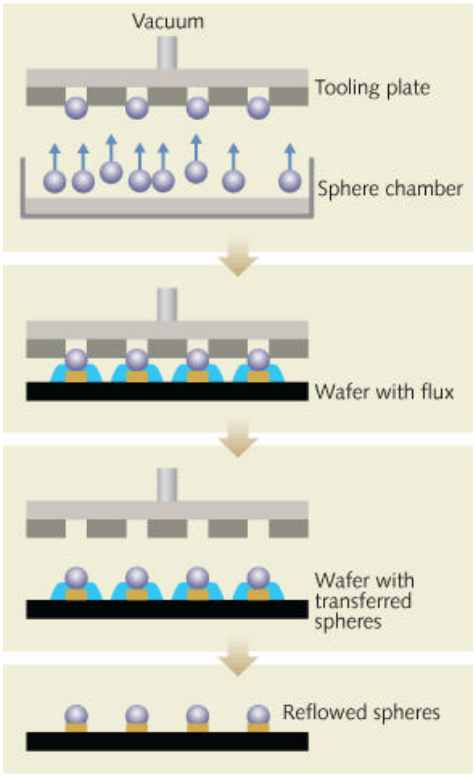

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Figure 1. Solder ball transfer process flow.

Solder Ball Transfer for Flip Chip and WLCSP

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(March 19, 2008) — Wafer bumping is often separated into two different categories: flip chip bumping and wafer-level chip scale packaging (WLCSP). This categorization and affiliated nomenclature is mainly based on solder bump size and the type of equipment used to create the bump. "Flip chip" refers to bumps on semiconductor wafers in the range of 50 to 200 µm in height. "WLCSP" refers to bumps that are in the range of 200 to 500 µm in height. Flip Chip bumps are traditionally created by electroplating, evaporation (C4), or paste printing; while WLCSP bumps are produced by dropping preformed solder spheres onto the wafer.

Pushing the limits of each of these technologies has allowed some overlap between these two bumping classifications. But for the most part, volume manufacturing of flip chip bumps and WLCSP bumps are carried out using different processes steps and different types of equipment. One new technology that is showing high promise toward completely bridging this technology gap is solder ball transfer (SBT).

SBT technology uses patterned vacuum tooling to simultaneously pick up preformed spheres and transfer them over to the wafer. **Figure 1** outlines the basic steps in the SBT process. First, a tooling plate is lowered into the sphere reservoir. Vacuum is applied to the tooling plate to selectively pick up the spheres. The tooling is then aligned to the wafer and lowered to bring balls into contact with the wafer pads. Finally, the vacuum is turned off; the tooling plate is raised; and the solder is reflowed.

The tooling plate is patterned with openings that correspond directly with the location of the I/O pads on

the wafer. This tooling is created using similar methods to that of making a nickel plated surface-mount stencil. The size of openings in the tooling is designed to be slightly smaller than the size of spheres that will be placed onto the wafer. Because this tooling plate can be made with such accuracy and because the SBT equipment has a placement accuracy of ±10µm, the process can be used for both WLCSP and flip chip applications.

Integration of Flip Chip and WLCSP Processes

When choosing one of the various bumping technologies (process flow and equipment) for creating solder bumps for either flip chip or WLCSP applications, several operations in addition to solder deposition should be considered. These include under-bump-metallurgy (UBM), fluxing, reflow, repair, cleaning, and inspection. For most of the traditional bumping technologies, these are discrete operations and require distinct and separate tools for each step. SBT combines several of these operations into a single tool that can lead to higher throughput and yields, and lower costs.

UBM is an integral part of all the bumping processes. Both aluminum-based and copper-based integrated circuits (ICs) require some interfacial material between the I/O pad and the solder bump. This material is typically deposited by either physical vapor deposition (PVD), electroplating, or electroless plating. All three are compatible with SBT bumping technology and are carried out as separate steps prior to the actual solder bumping operation.

The choice between the three UBM technologies is often dictated by cost and reliability. PVD and electroplating techniques require both high vacuum and photolithography steps and are therefore considered high cost operations. The electroless nickel/gold process technology is a simple wet chemical process that is self-patterning and is therefore low cost in relation to its total capital investment and operational costs.

The electroless nickel process is continuing to make inroads in the bumping industry not only because of low cost, but also because of high throughput and versatility (plating on either copper or aluminum based semiconductors). Recently, the electroless nickel/gold process has been shown to have additional advantage over the other UBM technologies in both mechanical and thermal reliability. The intermetallics formed between the solder and the electroless nickel have surpassed both the sputtered and electroplated technologies in drop testing, high-speed shear, high-speed pull, thermal cycling, and humidity testing.

Many of the remaining six process steps — fluxing, solder deposition, reflow, repair, inspection, and cleaning — can be carried out as part of the SBT operation. The SBT equipment can be configured in several different ways to match predominant bump size, preferred fluxing technique, and inspection criteria with other processes and equipment in the fab. For example, flux can be applied prior to ball placement by either screen-printing, stencil printed, or spin coating; or the SBT tool itself can be configured with a flux coating station to increase throughput. The tool can also be fitted with a hot plate reflow station, inspection capabilities, and a bump repair station.

Even though the SBT tool can perform both flip chip bumping and WLCSP bumping (100mm through 300mm wafers), the configuration of the tool is often dictated by the product line distribution (flip chip vs WLCSP volumes). For WLCSP applications, the added cost to integrate all six process steps into one tool might not be justified based on the expected yields and throughputs (30-45 wafers/hour). Wafers for WLCSP applications have relatively large spheres and relatively few interconnects compared to flip chip applications. For example, 300µm spheres have been placed on 200 mm wafers with 80,000 I/Os at yield losses of 10 ppm.

For flip chip applications, where high yields are an absolute requirement, integration of all these process steps may be critical to achieve this performance standard. It is common for high-end applications, such as microprocessors, to have hundreds of interconnects per die. Even small bump yield losses can translate into high die yield losses. The integration of the inspection and repair operations into the SBT tool makes sense for these applications.

The SBT process has exceptional properties relative to bump size range (60-75 µm), yield (10 ppm), and uniformity (5 µm variation), and has the additional advantage of being able to deposit a wide variety of solder alloys, including high melting solders like AuSn or high-lead alloys, and ternary alloys like SnAgCu. The cost of the spheres is the main criteria that affect the cost of bumping. Because the spheres are priced on a per sphere basis, the bumping cost increases linearly as the number of I/Os increase on a wafer. The cost of these spheres is expected to drop as the implementation of the SBT process expands.

Conclusion

The advantage of being able to deposit both flip chip and WLCSP sized bumps using the same equipment and same process flow will increase the implementation of wafer bumping. The SBT process offers a good alternative to many of other methods used to bump silicon wafers, such as electroplating, sphere drop, solder jetting, C4NP, and paste printing. Many of these other solder deposition processes have been practiced using varying degrees of automation. The SBT process is designed to run in either a semi-manual mode for prototyping or highly automated for high volume applications. When coupled with

an e-nickel UBM, the SBT technology can deliver the most versatile and lowest cost alternatives for bumping wafers. Continued innovation and volume implementation will make SBT a good alternative to other bumping technologies.

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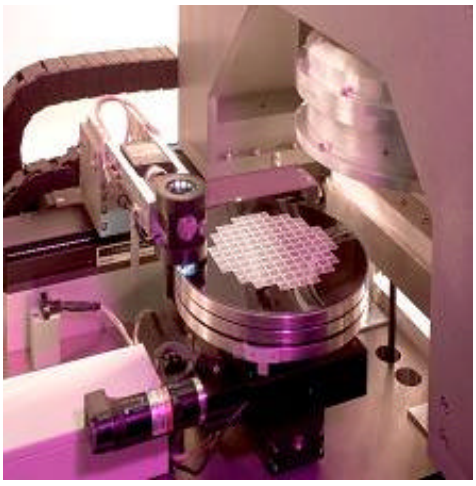

Figure 2. Close-up view of the SBT tool (PacTech Ultra-SB2).

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