Laser Based Assembly of Ultra Fine Pitch Bumped ICs
For
Chip-to-Chip Proximity Coupled Applications

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Solder Bumping Technologies
(Bump Size)

Most Common Deposition Techniques:
Paste Print, Electroplate, Sphere Drop, Sphere Transfer
Ultra Fine Pitch Bumps for: High Density Interconnects (x-y) - Close Proximity Applications (y)

3D Integration

- Die-on-Die
  - Memory-on-DSP
  - Passives-on-Die

Applications

- Memory-Stacking
- AC/DC - Coupled Stack

Applications

- High Speed RF
- Capacitive-Inductive

Requirements

- Chips and layout are different
- May require RDL

- Every chip the same

Fab

- Backend/WLP- Solder
- FE/Fab - TSV - TCB Cu
- DC current to all chips
- Close proximity

- Backend/WLP- Solder

Chips and layout are different
- May require RDL

- FE/Fab - TSV - TCB Cu
- Backend/WLP- Solder

StatChipPAC

- Samsung

NC State
Test Vehicle: 3 Chips ..... (2) Island – (1) Bridge

Properties/Requirements:
• Ultra Fine Bumps (<10 μm)
• FC Sized Bumps (~80 μm)
• 8 inch wafers (Island & Bridge)
• Ceramic Substrate (w/cavity)
• Thinned Die (150 μm)
• Mixed Solder Alloys
Bridge Chip

Specifications:
- 456 bond pads
- 40 µm bond pads
- 30 µm passivation opening
- 50 µm pitch
- x-y: < 5 µm resolution
- z: < 10 µm chip-to-chip spacing
- z: 150 µm die thickness
Island Chip

X: 15130 µm
Y: 12250 µm

Specifications:
- 456 Bond Pads that match Bridge Chip
- 2856 Flip Chip Bumps (70µm pads)
- ~ 80µm Bump Height
Three Chip Assembly

2 High Power Island Chips
1 Low Power Bridge Chip (<10W)

Proximity Coupled Communication
Low Power
High Bandwidth
Low Noise
High Density

Reference:
Process Overview:

1) Deposit Ni/Au UBM (Bridge and Island)
   3 µm

2) Bump Bridge Die (Sn)
   2-3 µm
   Bump Island Die (SnPb)
   ~80 µm

3) Thin & Dice Wafers
   150 µm

4) Die Laser Assembly
   (1-Bridge to 2-Island)

5) Substrate Laser Assembly
e-Ni/Au UBM

e-Ni/Au Process on Aluminum:

1) Passivation Clean
2) Aluminum Etch
3) Zincation I
4) Zinc Strip
5) Zincation II
6) Electroless Nickel
7) Immersion Gold

Wafer Level Wet Chemical Batch: 50 w/hr

PacLine-300™ PacTech

Images are not to scale relative to each other
Ni/Au Uniformity and Adhesion

Nickel/Gold uniformity across 8 inch wafer

Tall Nickel

Shear Analysis

70 µm octagonal flip chip pads

Average: 128.05
Max: 142.11
Min: 110.42
Std: 7.121
Mode: Al Fracture
Ultra Fine Pitch Solder Bumping (Bridge Die)

At IMAPS DPC 2009 reported 4 different technologies for lift off resist:

1) Three retro-resists
2) PMMA/Novolak stack

After presentation, person from audience came up and suggested alternative 3) Use standard positive resist, coat twice, flood expose first layer, and pattern expose second layer

Double Layer Resist Process

Deposit Resist 1 Flood Expose

Deposit Resist 2 Pattern Expose

Develop & Descum

Sputter Sn

Strip Resists
Tin Sputtering

Sn uniformity across 8 inch wafer

Chilled Plate Slow Sputtering

Smooth Sn on Liftoff Resist

Wrinkled Sn on Liftoff Resist

Sn Features on Bridge Die after Liftoff
Wetability and Reflow Tests

Oven Reflow at 265-285°C
Flux and Oven Reflow
Laser Reflow
Vapor Phase Reflow

3µm Sn on NiAu (misaligned)

1) Nothing happens
2) Variable pull back
3) Black film

Elemental analysis shows Sn is highly oxidized

Sputter thin Au layer on top of Sn (enabled by liftoff process) 500Å
Wetability and Reflow Tests

- **Oven Reflow w/Flux**
  - Solder moved completely onto the pads
  - Sn completely converted to Sn-Ni intermetallics

- **Laser Reflow No Flux**
  - Solder moved completely onto the pads
  - Pyramid shaped => Sn has not formed excessive IMC due to short pulse laser reflow

Pads Ni/Au and Sn/Au
Flip Chip Solder Bumping (Island)
2856 bumps/die

Prototyping  SB²™PacTech

Production  Ultra SB²™PacTech

Requirements:
• High Yield Bumping Process
• Bump Uniformity
• Reliable Interconnect
• ~80 µm Bump Height (100 µm spheres)
• SnPb Eutectic
Flip Chip Bumped Die  (SnPb Eutectic - 2856 bumps/die)

**Bump Height**
Ave: 84.93
σ: 0.78
3σ: 2.35

**Shear Force**
Ave: 32.04
σ: 1.27
Cpk: 4.46
Failure Mode: Ductile Solder
Laser Assembly

1) Pickup Die & Align
   (±5 µm)

2) Contact
   (10kgf)

3) Laser Reflow
   (20msec, Nd³YAG)

LaPlace Assembly System™ PacTech

Placement accuracy: +/- 15um: 3000 - 5000 UPH
Placement accuracy: +/- 10um: ~2000 UPH
Placement accuracy: +/- 5um: ~1000 UPH
Placement accuracy: +/- 2.5um: ~500 UPH

Laser based assembly allows localized heating:

- Selective to individual die
- Energy localized to bumped areas
- Ability to differentiate between solder alloys
- Low stress
- Minimizes IMC (time/temp)

Mp SnPb = 183°C  Mp Sn = 232°C
Assembly Process Steps:

1. Pick up Bridge Chip
2. Align Bridge Chip to first Island Chip
3. Bond Bridge Chip to first Island Chip by Laser Reflow
4. Pick up bonded Bridge-Island combination
5. Align Bridge-Island assembly to second Island Chip
6. Bond Bridge-Island combination to the second Island Chip by Laser Reflow
7. Pickup three chip assembly
8. Align to substrate
9. Bond Island-Bridge-Island combination to substrate by Laser Reflow
Joint Integrity Tests

- No Shorts Observed
- No Opens Observed
- Good wetting on both Bridge and Island after disassembly

Bridge Die

Island Die
Conclusions:
• Liftoff process versatile technique for creating ultra fine pitch Sn solder bump
• Au cap on Sn is essential for good wettability and reflow characteristics
• Laser reflow enables assembly of ultra fine pitch Sn bumps (minimizing IMC)

Ongoing Work:
• Variation in laser assembly energy, pulse width, contact force,…
• Substrate cavity machining (Ceramic and Laminate)
• FlipChip laser assembly to substrate
• Electrical & Capacitive signal transmission analysis
• Underfill studies
• Cross-section analysis of solder joints and intermetallics
• Variation in chip-to-chip spacing (e-Nickel thickness)