Processing and Reliability Analysis of Flip-Chips with Solder Bumps Down to 30 µm Diameter

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Abstract
The accelerated trend to smaller and lighter electronics has accentuated many efforts towards size reduction and increased performance in electronic products. However, equipment and processes of electronics production have to come along with this trend when it comes to connections on board level. The use of flip-chip bonding technology employing micro bumps for very fine pitch packaging is becoming increasingly important in the microelectronics industry. To meet these requirements, cost-efficient solder bumping and automated assembly technologies for the processing of flip-chips have been developed and qualified. Flip-chips used in this study show a pitch of 100 µm and solder ball diameter of 40 µm and 30 µm, respectively.

Wafer level solder application has been done using wafer level solder sphere transfer (WLSST) process and solder sphere jetting (SB²) technology, respectively. The latter is a technique that has been used for many years in the wafer level packaging industry and is commonly known as a solder ball bumping tool. For the described work the SB² technology was scaled down for processing solder spheres with diameters of 30 µm with very good results achieved. Our research has shown that the underfill process is one of the most crucial factors when it comes to flip-chip miniaturization for high reliability applications. Therefore, a total of thirty different underfill materials were investigated initially in terms of flow time, gap height, filler sedimentation, and reliability.

For reliability investigations, various standardized test conditions were applied to the test specimen. In previous experiments we found out that solder spheres of 50 µm seem to be the technological limit with current organic printed circuit board technology with subtractive structuring. Therefore, thin film ceramic as substrate material has been used showing excellent performance of the highly miniaturized solder joints at several reliability tests. Concluding long-term reliability and an analysis of the intermetallic growth are shown using SEM/EDX. Additionally, an analysis of the failure mechanism will be presented and recommendations for further miniaturization will be outlined.

Advantages of the developed technology are lower cost compared to known techniques, very high flexibility and freedom in selection of solder composition including SAC, low melting alloys, gold-tin, and further special alloys.

Introduction
Production of flip-chips with solder bumps of 80 µm diameter was state of the art at the beginning of the project using WLSST technology. Processing of solder spheres with 60 µm, 50 µm, or 40 µm done by the authors is already described in [6] and [24]. Aim of the investigations was to develop a process chain for flip-chips with solder spheres down to 30 µm diameter using standard SMT production equipment. This includes structuring and use of organic FR4 and BT substrates as well as thin film ceramic for fine pitch applications, qualification of an adapted wafer bumping process as well as automated assembly and underfilling of silicon dies with conventional equipment. Thereby a flexible and very cost-effective production even of small quantities throughout the process chain has been facilitated.

The advantages of flip-chip technology like size reduction and cost saving potential made it one of the most attractive techniques for highly miniaturized electronic devices. Further miniaturization leads to higher I/O density and reduction of the pitch with increasing requirements on production systems.

Since the development of one of the first bumping techniques still in industrial use, called C4 (Controlled Collapse Chip Connection [5]), many bumping processes have been established in recent years. Common methods for applying solder onto the semiconductor wafer are for example stencil printing [20], electroplating [11][13], Controlled Collapse Chip Connection New Process (C4NP) [4], solder jetting [35] and WLSST process [27]. For all bumping processes, the most important requirements are fast processing with high yield and cost efficiency as well as low tooling costs. The latter two processes have been used during the experiments described in this paper.

Design of flip-chip and test specimen
For all experiments, the same silicon chip layout has been used. The flip-chip has a thickness of 0.8 mm and side lengths of 10 mm. The solder spheres are made of a SnAgCu alloy and are placed on a NiAu UBM realized in an electroless nickel process. Each row has a different passivation opening for solder spheres measuring between 60 µm (first row), 50 µm (second row), 40 µm (third row), and 30 µm (fourth row) which is shown in Figure 1. I/O-count is dependent on the solder sphere size – for example 360 I/Os for 40 µm spheres, 354 I/Os for 30 µm spheres. 277 dies are placed on one wafer making it per wafer 99,720 I/Os or 98,058 I/Os, respectively, for 40 µm spheres or 30 µm spheres, respectively. In order to detect failures during the reliability tests, each die has a circumferential daisy chain structure.

The flip-chip and PCB structures are realized in a way that one layout can be used for chips with 60 µm, 50 µm, 40 µm or 30 µm solder spheres. The daisy chain connection is integrated for each of the solder sphere sizes and each chip can be connected for online measurements during reliability testing.
Figure 1. Upper part: Layout of the flip-chip. Lower part: Magnification of the passivation openings (with solder spheres applied at the 30 µm row) and single solder sphere with a diameter of 30 µm.

Two different kinds of substrates were used for the experiments. On the one hand it was the aim of the substrate structuring, that standard processes of the subtractive PCB technology can be used. This meant that for passivation reasons a solder mask had to be applied after etching the circuitry. As a surface finish ENIG has been used. The layout is shown in Figure 2 on the left side. Those kind of substrates can be used as cost-efficient interconnect structures for fine pitch applications.

As could be shown in [6], [8], and [24] the solder mask seems to have a negative effect on the long term reliability of the solder joints, when solder spheres with a diameter smaller than 50 µm are used. Because of this, a second test specimen based on thin film ceramic technology has been used, in order to overcome the limitations of the solder mask. The layout is shown in Figure 2 on the right side. As can be seen, the wettable areas of the thin film ceramic substrate are of high precision.

FR4 Thin film
Solder mask Metallization 40 µm Pads 30 µm Pads
100 µm 100 µm

Figure 2. Layout of FR4 and thin film ceramic substrates.

Wafer Bumping Process

Several techniques exist for wafer level solder bumping including paste printing, electroplating, or solder sphere placement. In this study, two different techniques have been evaluated: A wafer level solder sphere transfer (WLSST) process which places all solder spheres onto the wafer at once [24][26][27][30] and a laser based bumping process which drops a single solder sphere onto the bond pad and then laser reflows the solder just as it reaches the pad [1][12][21][35].

The first solder bumping method used in this study places all the solder spheres at once onto the wafer using a solder sphere transfer technology. This technique is more relevant for higher volume applications where cost and throughput are critical. The basic principle of this technology is to simultaneously pick up preformed solder spheres using a patterned vacuum plate and then accurately place them onto the bond pads of the wafer.

This technique requires a tacky flux to be applied to the wafer prior to bumping. This flux acts both as a medium to hold the solder spheres in place until it is moved over to a reflow station, but also as a wetting agent for the solder. Preformed solder spheres with diameters down to 40 µm are compatible with this WLSST technology.

The second solder bumping method which was used, the laser based single-sphere process, has no mechanical contact with the wafer and is fluxless, thus eliminating any chemical interactions with the device or need for protective resists. Solder bumps using this technique are deposited at a rate of 6 to 8 spheres per second.

This technology has been used successfully for many applications but is most useful for low volume products, prototyping or products with low I/O count. Preformed solder spheres in the range of 50 µm to 760 µm are compatible with this technology and used for volume production in the
industry today. All solder alloys can be deposited with this system by adjusting the laser power and pulse width. Within this study the capability of depositing lead-free SnAgCu (SAC305) solder spheres with diameters of 30 µm was successfully proven as shown in Figure 1. Details can be found in [22].

Selection and qualification of underfill

The reliability of flip-chip interconnections depends on the components used in the set-up. Different values for the coefficient of thermal expansion (CTE of silicon die, substrate, and solder) cause thermally induced stress in the solder joint potentially leading to cracks. The use of underfill can reduce shear strain in solder joints between 75 % and 90 % according to [16][18][29]. To name only a few, modulus and CTE of the underfill, filler particle size and content, chip size, I/O layout, surface energies, gap height, voids and flux residues significantly influence the quality of the underfilled components [3][8][19][32][33][36].

<table>
<thead>
<tr>
<th>Underfill</th>
<th>CTE in ppm/K</th>
<th>Min. gap/Particle size in µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFU B</td>
<td>45</td>
<td>Gap: 12.7</td>
</tr>
<tr>
<td>CFU C</td>
<td>27</td>
<td>Gap: 25</td>
</tr>
<tr>
<td>CFU D</td>
<td>28</td>
<td>Gap: 25</td>
</tr>
<tr>
<td>CFU E</td>
<td>33</td>
<td>Particle: &lt;12</td>
</tr>
<tr>
<td>CFU G</td>
<td>28</td>
<td>Particle: ≤4</td>
</tr>
</tbody>
</table>

Table 1. CTE and particle size of the underfills investigated.

The five capillary flow underfills (CFUs) selected for the flow experiments (see Table 1) were chosen according to the material properties suggested in [18]. CTE and particle size or fillable gap height, respectively, were of special interest. With respect to the values from the data sheet, all five underfills should be able to fill gaps resulting from a solder sphere diameter of 40 µm. Underfills B, E and G seem to be sufficient for gaps resulting from solder spheres with a diameter of 30 µm.

At first, flow behavior of the five underfills in dependence of gap height and temperature had been under examination. Therefore, the dispensing temperature had varied between 90 °C and 120 °C in 10 K steps. The result is the optimum temperature for underfill application in order to realize a fast (no gelling) and void free underfill process due to reduced viscosity of the underfill material [2]. The ability to fill even small gaps between substrate and flip-chip surface is determined and analyzed by a variation of the gap height between 17 µm and 70 µm.

The set-up of the experiment is shown in Figure 5. A glass slide 10 mm by 10 mm in size was used to secure a good underfill by inspecting the process for voids and shape of the frontline of the underfill material during flow process. The defined gap height was realized by etched copper structures on the FR4 test specimen. The application of the underfill was done using an automated dispensing system. A dot of underfill was applied to the middle of one side of the glass chip.

First of all it can be stated, that all five underfills fill gaps as small as 17 µm. Exemplary the results for Underfills B, C and G are shown in Figure 5. Both underfills D and E show very good flow behavior which is independent from gap height. The fastest flow time shows underfill B even for gaps of 17 µm. But as reliability experiments described in [24] have shown, the pretty high CTE of CFU B has crucial influence on the long term reliability of the solder joints. Both, temperature and gap height have a strong influence on the flow time of underfill C and underfill G, although the particle size of CFU G is significantly smaller. The best process temperature seems to be at approximately 110 °C.

Cross section views of all underfills have been conducted to analyze the distribution of filler particles in the gap between chip and substrate. Exemplary, cross section views of CFU C and G are shown in Figure 6. A distinct sedimentation of particles can be seen for underfill C, whereas the filler particles of CFU G are equally distributed in the gap. Sedimentation can result from differences in the density of the sediments and the fluidic matrix as described in [10].

Figure 5. Flow time of underfills with respect to gap height and temperature. [25]

Figure 6. Cross section views. [10]
caused mainly by electro migration. Details can be found in the literature [14][17][28][34].

<table>
<thead>
<tr>
<th>Test No.</th>
<th>Method</th>
<th>Description</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EIA/JESD22-A101-B</td>
<td>Voltage between two daisy chains</td>
<td>85 °C/85 % r. humidity, 3 V</td>
</tr>
<tr>
<td>2</td>
<td>EIA/JESD22-A101-B</td>
<td>Life test, with current through the daisy chain</td>
<td>85 °C/85 % r. humidity, 100 mA</td>
</tr>
</tbody>
</table>

Table 2. Test methods used for underfill qualification.

The results for both tests are described in detail in [6], CFU C and G pass both tests. To summarize the results: Only underfills C and G meet all requirements regarding underfill selection. For further experiments, only CFU G has been used because of its better flow properties in small gaps.

Flip-Chip Assembly

Besides the necessity of manufacturing very fine pitched bumps in order to cope with steady miniaturization, the production processes for assembling flip-chips onto substrates were improved as well. Assembly machines used in high throughput production lines have to meet the needed placement accuracy as well and the vision systems have to detect the highly miniaturized bumps with high reliability. For the automated assembly process a machine with a placement accuracy of ±10 µm @ 3s has been used.

Substrate structures that are eligible for solder bump sizes below 50 µm were only realizable with thin film technology, which is very cost-intensive. Limitations of the subtractive PCB technology are described in [6] and [8]. We found, that the thickness of the solder mask of about 15 micron, the tolerances of the openings in the solder mask, and the tolerances of the solder mask registration are major drawbacks for a high assembly yield [7].

Figure 8 shows a cross section of a flip-chip with 40 µm solder spheres on a FR4 PCB. The tolerance of the solder mask registration caused the misalignment and irregular shape of the solder bumps. Based on our results, we observed a technological limit for flip-chip assemblies using PCB in subtractive structuring technology for solder spheres at 50 µm.

Additionally, Temperature Humidity Bias Tests (THBT) have been performed for the underfills. Here the test coupons are exposed to increased temperature and humidity (85 °C/85 % r. h.), whereby at the same time a bias of 3 V is applied to adjacent daisy chains. This experiment was performed in order to test the insulation resistance of the underfill material. A test with an applied current of 100 mA per chip was conducted as well in order to study effects
interconnections with solder sphere diameters of 40 µm or 30 µm are shown in Figure 9 to Figure 12. It can be seen, that solder joints of good regular shape can be realized on thin film ceramic.

Figure 9. Cross section of a test coupon with a chip with 40 µm solder spheres on thin film ceramic after reflow and underfill, showing the daisy chain structure.

Figure 10. SEM image of a cross section of a flip-chip with 40 µm solder spheres on thin film ceramic after reflow and underfill.

Figure 11. Cross section of a test coupon with a chip with 30 µm solder spheres on thin film ceramic, showing the daisy chain structure after reflow and underfill.

Figure 12. SEM image of a cross section of a flip-chip with 30 µm solder spheres on thin film ceramic after reflow and underfill.

Reliability testing

Reliability testing was performed according to the test methods given in Table 3. Temperature cycling was done according to MIL-STD 883G, method 101.8, condition B for over 8,000 cycles for test specimen with 40 µm solder spheres and 1,000 cycles so far for tests specimen with 30 µm solder spheres. Some parts were stored at 125 °C for 1000 hours. As failure criteria we defined for both tests an increase of the electrical resistance of the daisy chain of more than 20 percent.

<table>
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<th>Test No.</th>
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<th>Description</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>MIL-STD 883G, meth. 1010.8, c. B</td>
<td>Temperature cycling</td>
<td>-55 °C/+125 °C</td>
</tr>
<tr>
<td>4</td>
<td>MIL-STD 883G, meth. 1005.8</td>
<td>Dry heat storage</td>
<td>+125 °C/1000 hours</td>
</tr>
</tbody>
</table>

Table 3. Test methods used for reliability testing.

No failures could be found during dry heat storage. Flip-chip interconnections with a solder sphere diameter of 40 µm show early failures and a steady increase of the failure rate on PCB substrates during temperature cycling. This is due to the tolerances of the solder mask as described in the previous chapter and in [7].

Figure 13 shows the temperature cycling results for flip-chips with 40 µm solder balls on thin film ceramic according to MIL-STD 883G, method 1010.8, condition B. Even after 8,000 temperature shock cycles only one interruption of a single daisy chain (after 4,268 cycles) could be observed.

Figure 14. Failure rate of flip-chips with 30 µm solder bumps on thin film ceramic in dependence of the number of temperature cycles (-55 °C/+125 °C).
Further tests on the reliability of solder spheres with a diameter of 30 µm are still in progress.

**Results of the SEM/EDX Analysis**

Figure 15 shows a SEM image of a solder contact between thin film ceramic and chip after reflow soldering and underfill (top) and after 1,000 hours dry heat storage at 125 °C (bottom). No cracks are visible. The EDX investigation revealed that there is still ductile solder material between the intermetallic layers adjacent to chip and PCB metallization, which benefits the reliability according to [9].

![SEM image of a solder contact](image)

Figure 15. SEM image of a cross section of a flip-chip with 40 µm solder bumps on a thin film ceramic substrate after reflow soldering (top) and 1,000 hours dry heat storage at 125 °C (bottom). P1 to P5 are measurement points for EDX analysis.

P2 characterizes an intermetallic compound formed from Ni and Au (from the metallization of the thin film ceramic). P4 represents an intermetallic compound formed from Ni and Sn. The most important measuring point is P3, which shows that ductile solder is still present in the solder joint.

Figure 16 shows an element mapping for a solder joint formed from a solder sphere of 30 µm in diameter. Significant but typical for SnAgCu solder is the large precipitation (most likely Ag3Sn) at the left side of the solder joint.

Figure 16. Element mapping of a solder connection with 30 µm bump for the elements Ni (red), Sn (green), Ag (blue), and SE-Image.

![Element mapping](image)

Figure 17. SEM picture with measurement points P1 to P6 for EDX analysis after reflow soldering.

The measurement points of the EDX-analysis for a solder sphere with 30 µm diameter after reflow soldering and underfill are shown in Figure 17. P2 characterizes an intermetallic compound formed from Ni and Au (from the metallization of the thin film ceramic). P4 represents an intermetallic compound formed from Ni and Sn. The most important measuring point is P3, which shows that ductile solder is still present in the solder joint. A cross sectional view of a solder joint with 30 µm solder sphere diameter after 1,000 temperature cycles (-55 °C/+125 °C) in Figure 18 indicates that ductile solder still is present, confirmed by EDX analysis.

![Cross section view](image)

Figure 18. Cross section view of a 30 µm solder joint after 1,000 temperature cycles. No cracks could be found.

**Discussion**

When discussing the results of flip-chip assembly and reliability testing for solder spheres diameters of 40 µm and 30 µm, underfill and substrate material are the most crucial factors. The interruptions of the daisy chain of chips with 40 µm solder bumps on PCB could be traced back to PCB tolerances, especially of the solder mask registration. Variations from the nominal dimensions of the opening in the
solder mask and their tolerances in position lead to solder joints of irregular shape which is conducive to an uneven strain distribution in the solder joints causing cracks during temperature cycling. Additionally, openings in the solder mask are prone to voids in the underfill that have a negative impact on reliability of the assembly. The solder mask height of 15 µm is clearly the limiting factor for the assembly of flip-chips with solder spheres of 30 µm in diameter on PCBs.

The lack of a thick solder mask at the thin film ceramic substrates is very advantageous: The larger gap between chip and substrate surface guaranties a perfect flow of the selected high performance underfill. No voids could be found. This has been conducive for the reliability tests, where only one failure occurred for 40 µm solder spheres after 4,268 temperature cycles and no additional defect up to 8,000 temperature cycles or zero failures after 1,000 cycles for 30 µm solder spheres, respectively.

Conclusions

Results of an extensive experimental study on the assembly process of flip-chips with 40 µm and 30 µm solder spheres have been presented in this paper. On the one hand, it was possible to demonstrate automated flip-chip assembly of bumped chips and a reliable underfill process with the given solder sphere diameters. Additionally, package level reliability test results for assembled test specimen could be shown. Some important results are summarized as follows:

1. A flip-chip assembly technology has been demonstrated for chips with 40 µm and 30 µm solder spheres, respectively, using thin film ceramic.

2. PCBs in state of the art subtractive technology impose restrictions to further miniaturization of solder bump size at 50 µm.

3. In comparison, assembly and underfill process of flip-chips with 40 µm or 30 µm solder spheres on thin film ceramic have been also studied. We found that the yield and reliability results are much better than those obtained with PCBs.

4. The flip-chip assemblies have passed the required reliability tests.

5. Additional work is on the way in order to increase the assembly yield and to prevent early failures.

The innovations in flip-chip technology will help to meet the demands of packaging for next generation medical [31], mobile [23] and microwave applications. Fluxless flip-chip assembly is in demand especially for medical and optoelectronics packaging [15] and can be done using slightly modified process steps, which is subject of future publications. Our technology is well suited for silicon die stacking and for 3-D packaging [11][15].

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